

Efficient Computing for AI and Robotics

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Slides available at

<https://tinyurl.com/SzeMITDL2020>

Processing at “Edge” instead of the “Cloud”



Communication



Privacy



Latency

Computing Challenge for Self-Driving Cars

JACK STEWART TRANSPORTATION 02.06.18 08:00 AM

SELF-DRIVING CARS USE CRAZY AMOUNTS OF POWER, AND IT'S BECOMING A PROBLEM



Shelley, a self-driving Audi TT developed by Stanford University, uses the brains in the trunk to speed around a racetrack autonomously.

NIKKI KAHN/THE WASHINGTON POST/GETTY IMAGES

WIRED

(Feb 2018)

Cameras and radar generate
~6 gigabytes of data every 30 seconds.

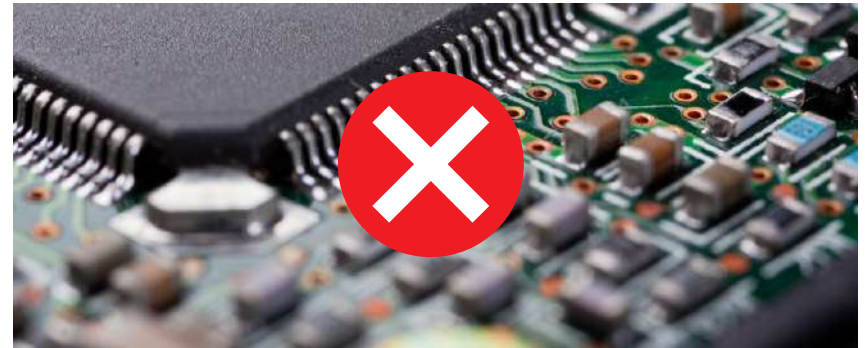
Self-driving car prototypes use approximately 2,500 Watts of computing power.

Generates wasted heat and some prototypes need water-cooling!

Existing Processors Consume Too Much Power



< 1 Watt



> 10 Watts

Transistors are NOT Getting More Efficient

Slow down of Moore's Law and Dennard Scaling

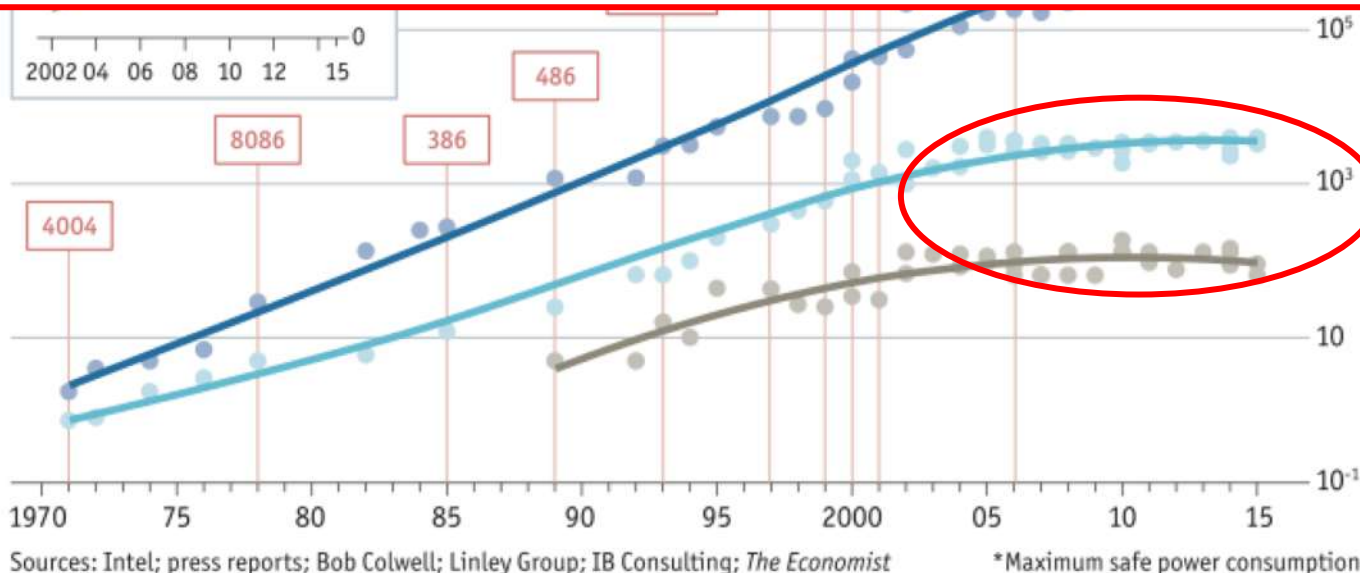
General purpose microprocessors not getting faster or more efficient

Stuttering

● Transistors per chip, '000 ● Clock speed (max), MHz ● Thermal design power*, w

□ Chip introduction dates, selected

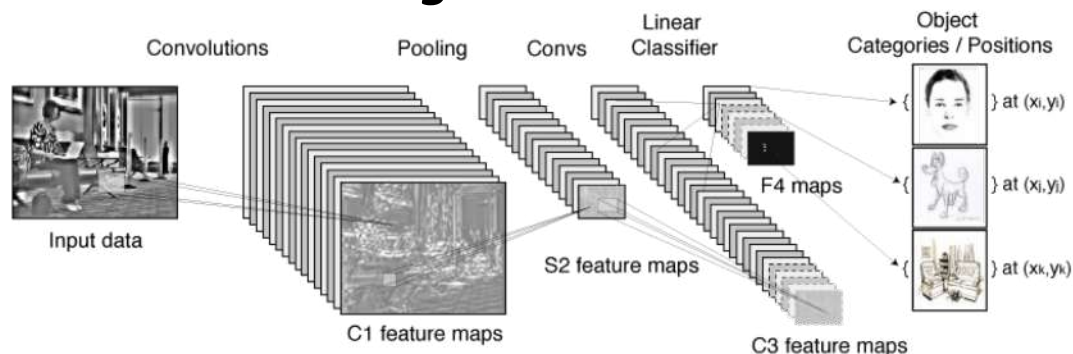
- Need **specialized hardware** for significant improvement in speed and energy efficiency
- **Redesign computing hardware from the ground up!**



Slowdown

Energy-Efficient Computing with Cross-Layer Design

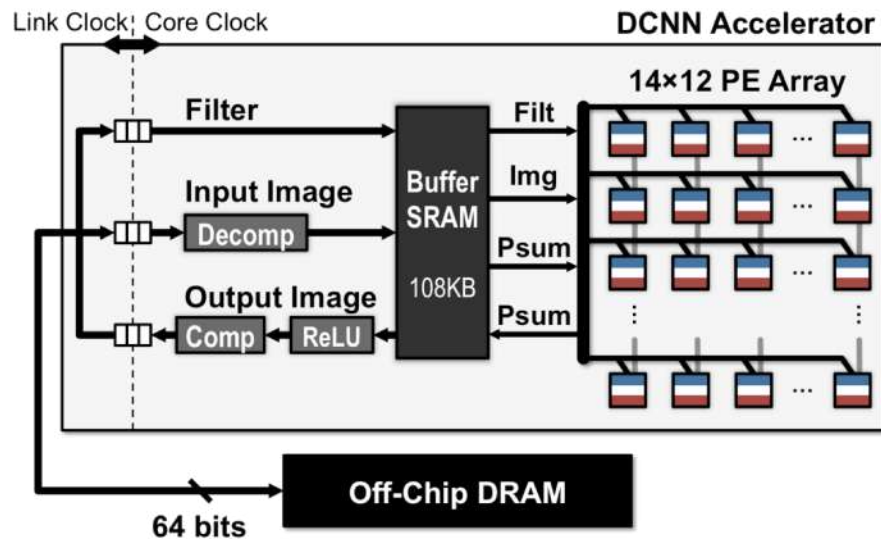
Algorithms



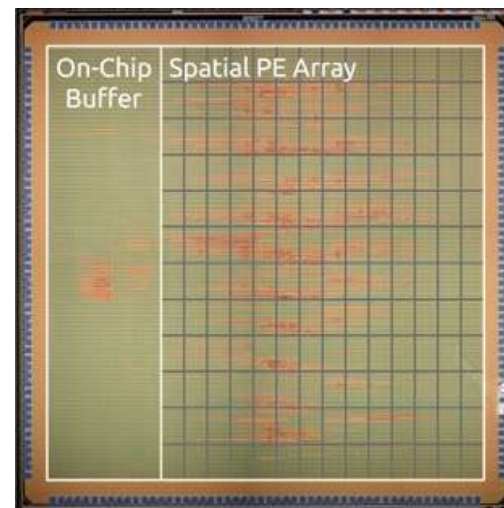
Systems



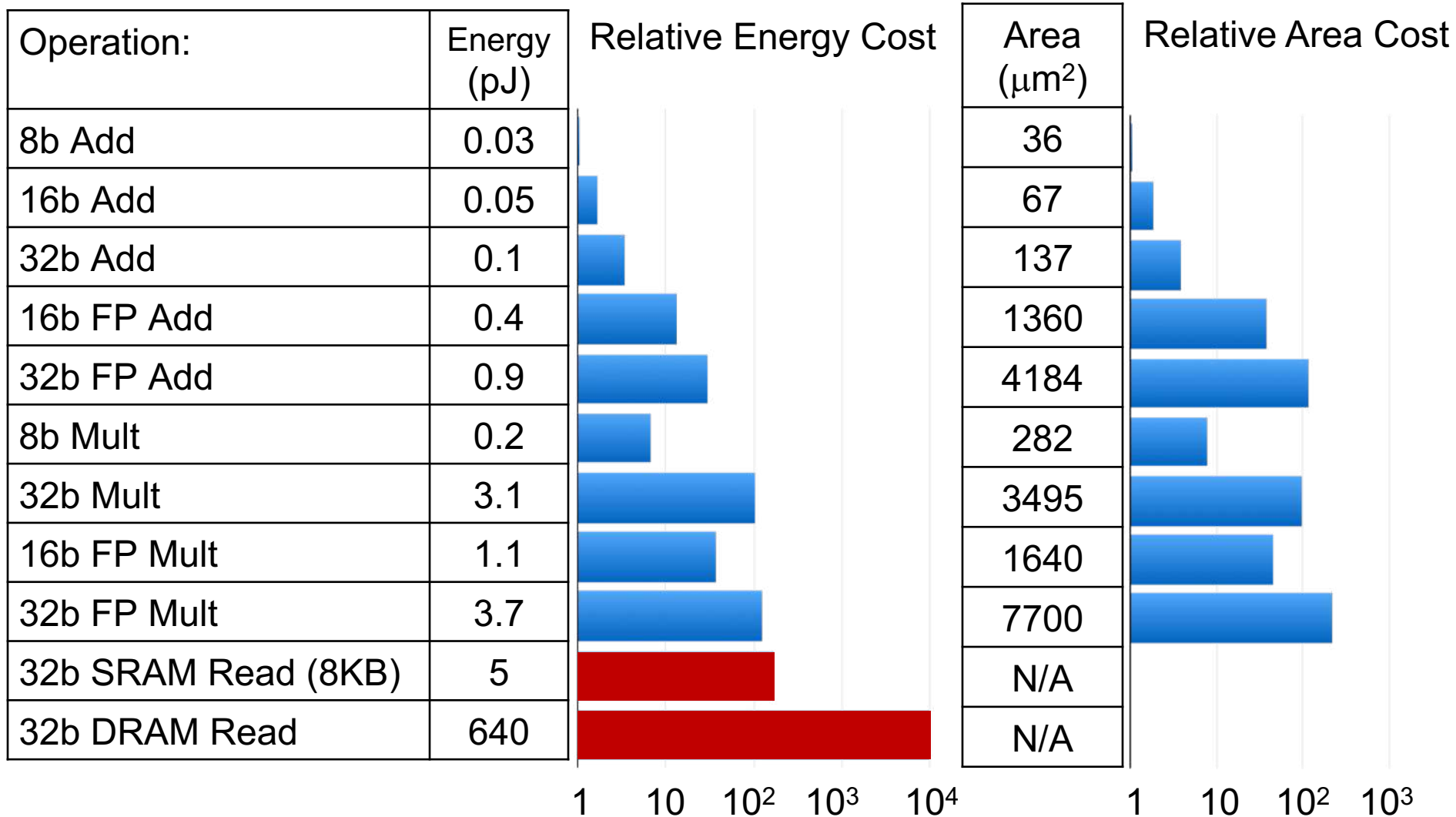
Architectures



Circuits



Power Dominated by Data Movement



Memory access is **orders of magnitude** higher energy than compute

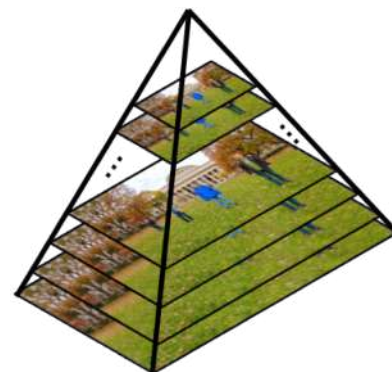
Autonomous Navigation Uses a Lot of Data

- **Semantic Understanding**

- High frame rate
- Large resolutions
- Data expansion



2 million pixels



10x-100x more pixels

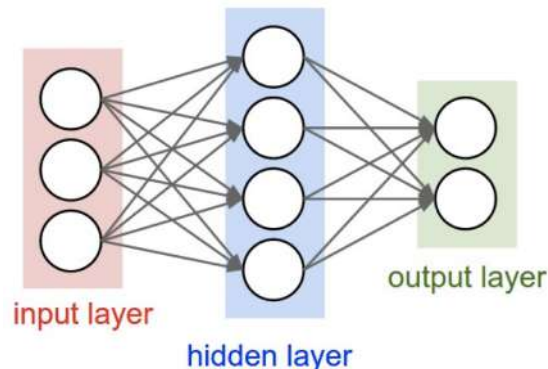
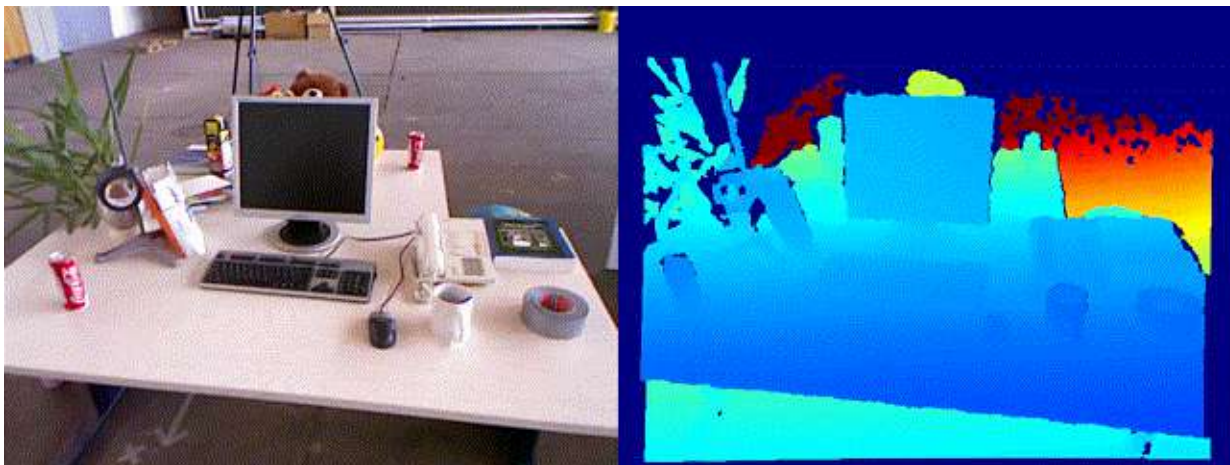
- **Geometric Understanding**

- Growing map size

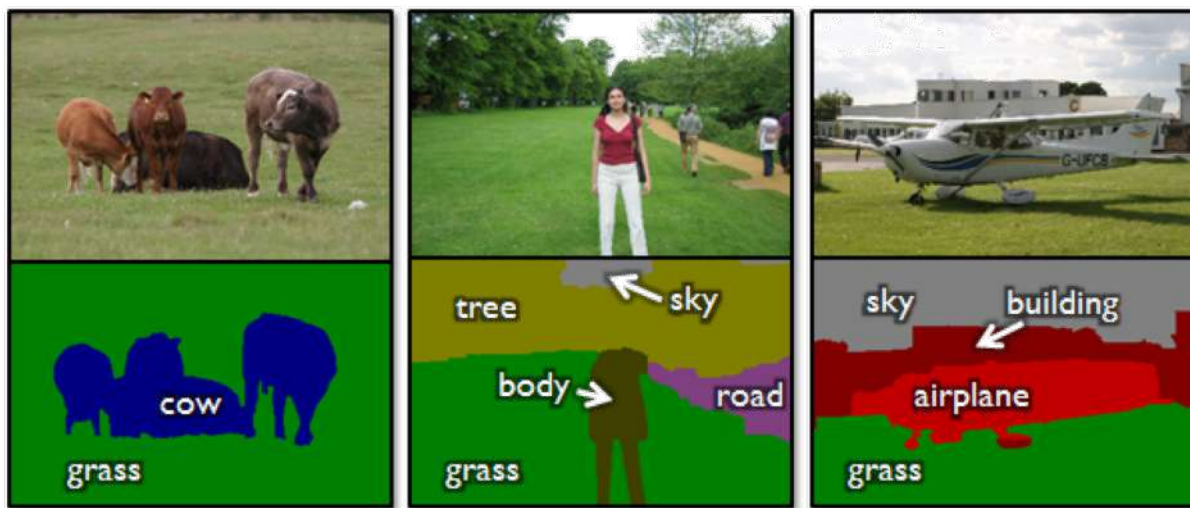


Understanding the Environment

Depth Estimation



Semantic Segmentation



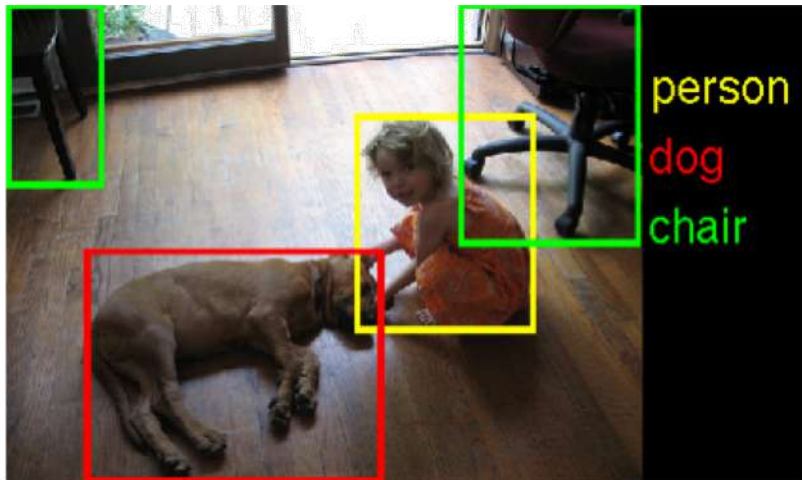
State-of-the-art approaches use **Deep Neural Networks**, which require **up to several hundred millions of operations and weights to compute!**

>100x more complex than video compression

Deep Neural Networks

*Deep Neural Networks (DNNs) have become a **cornerstone of AI***

Computer Vision



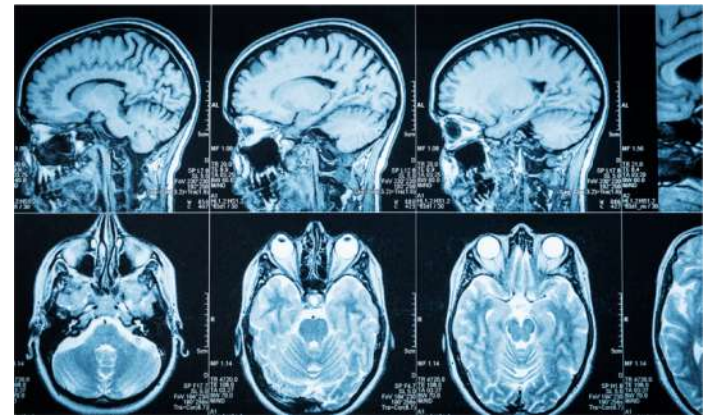
Speech Recognition



Game Play

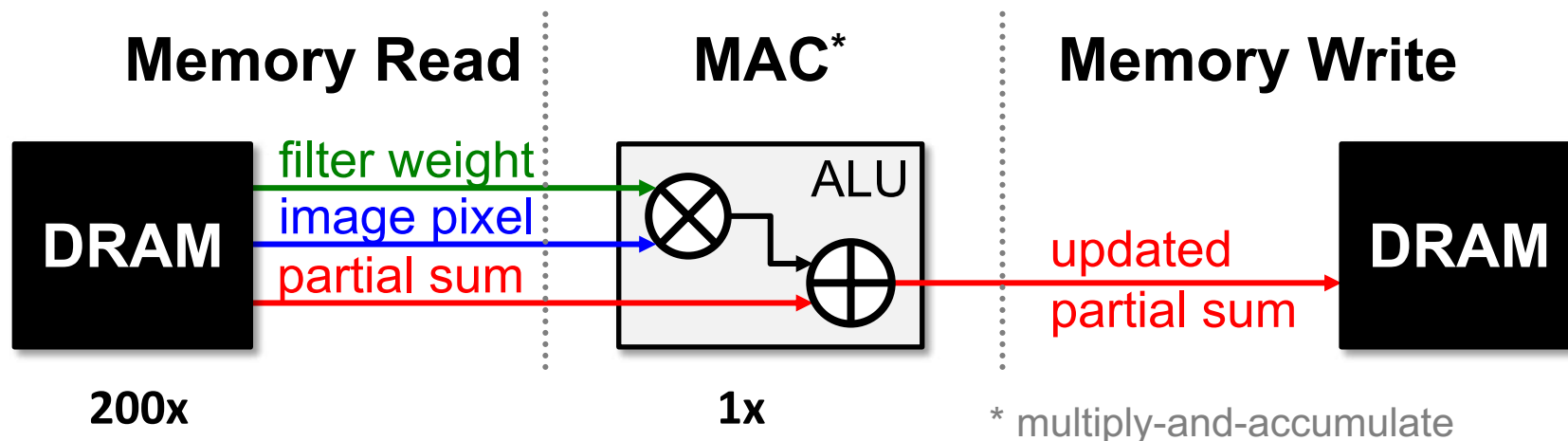


Medical



Properties We Can Leverage

- Operations exhibit **high parallelism**
→ **high throughput** possible
- Memory Access is the Bottleneck

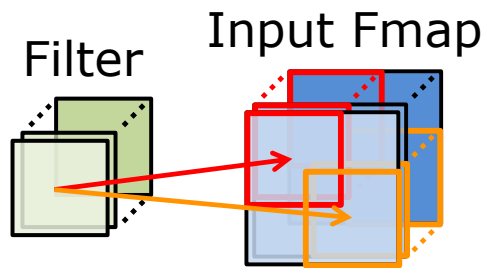


Worst Case: all memory R/W are **DRAM** accesses

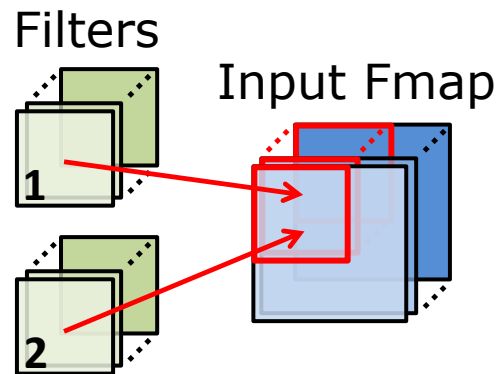
- Example: AlexNet has **724M** MACs
→ **2896M** DRAM accesses required

Properties We Can Leverage

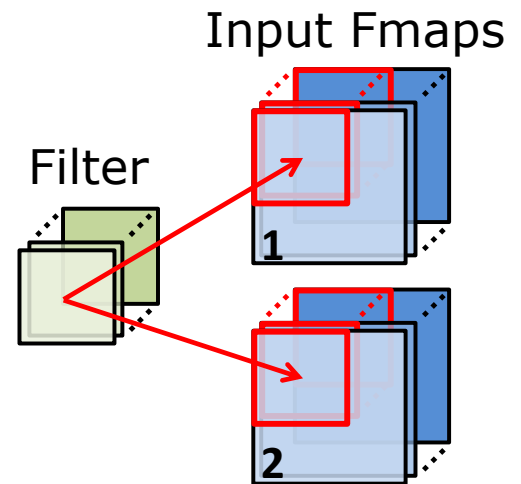
- Operations exhibit **high parallelism**
→ **high throughput** possible
- Input data reuse** opportunities (up to 500x)



Convolutional Reuse
(Activations, Weights)
CONV layers only
(sliding window)

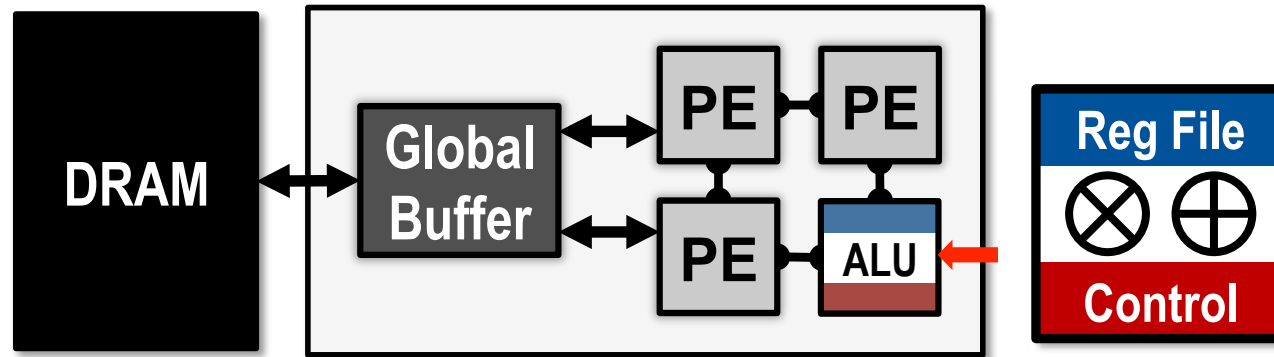


Fmap Reuse
(Activations)
CONV and FC layers

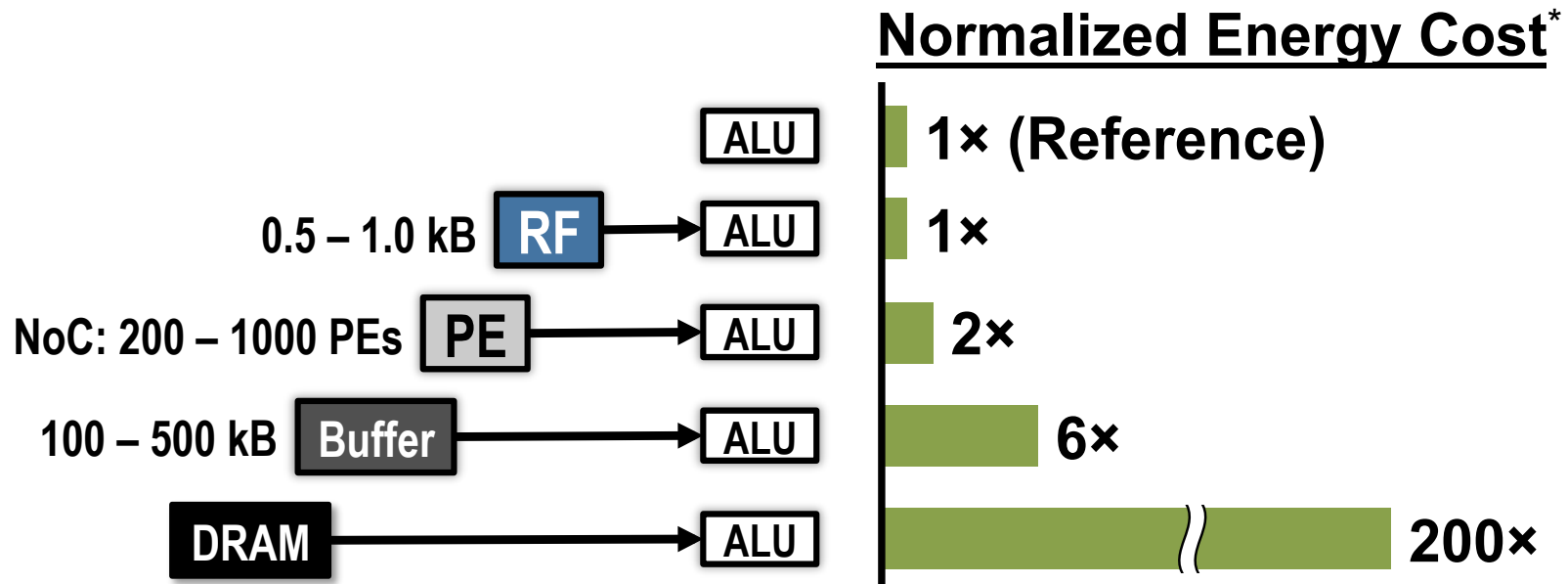


Filter Reuse
(Weights)
CONV and FC layers
(batch size > 1)

Exploit Data Reuse at Low-Cost Memories



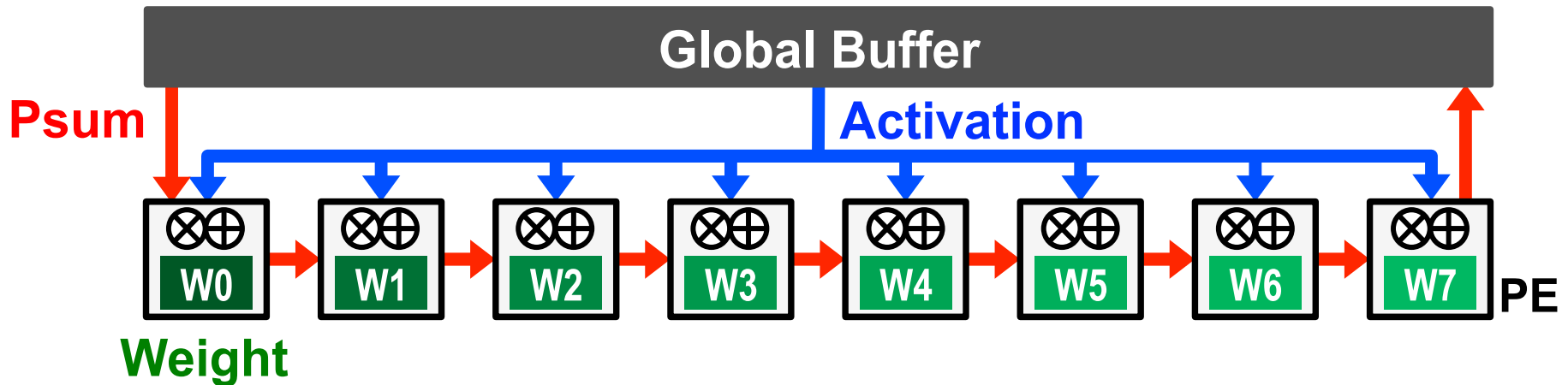
Specialized hardware with small (< 1kB) low cost memory near compute



* measured from a commercial 65nm process

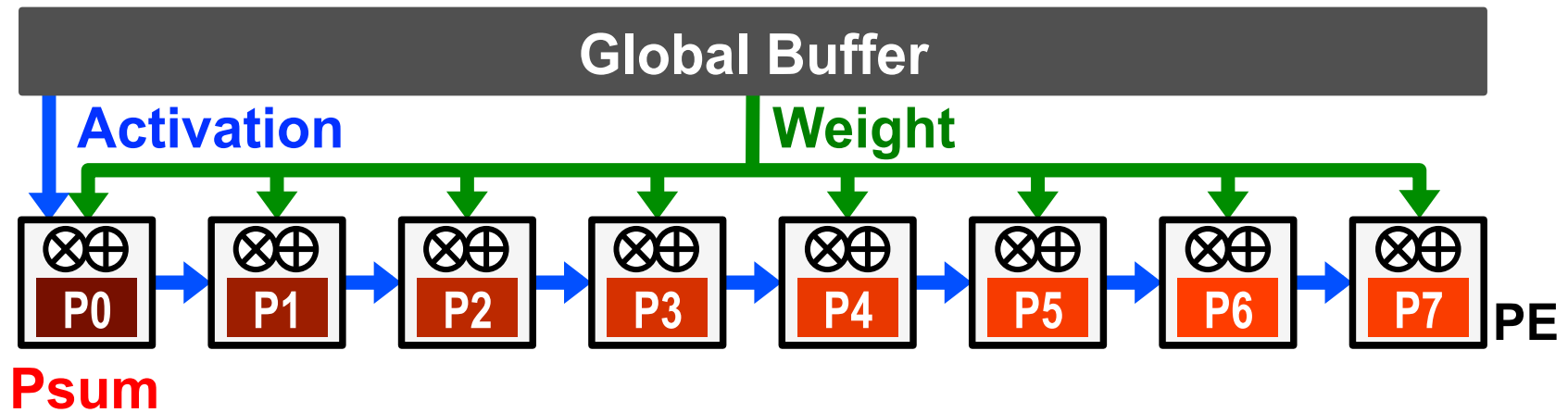
Farther and larger memories consume more power

Weight Stationary (WS)



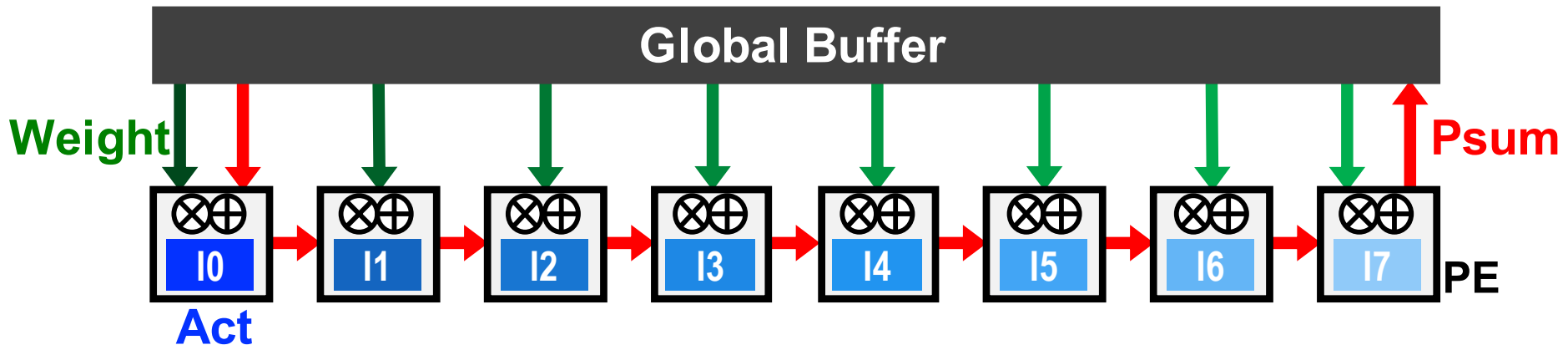
- **Minimize **weight** read energy consumption**
 - maximize convolutional and filter reuse of weights
- **Broadcast **activations** and accumulate **partial sums** spatially** across the PE array
- Examples: **TPU** [Jouppi, ISCA 2017], **NVDLA**

Output Stationary (OS)



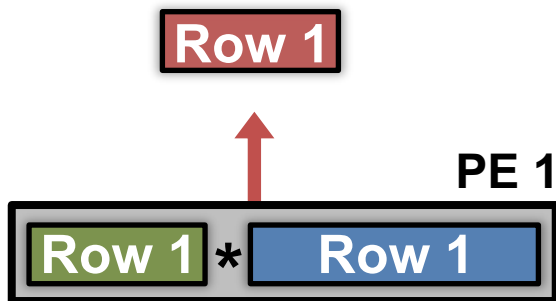
- Minimize **partial sum** R/W energy consumption
 - maximize local accumulation
- Broadcast/Multicast **filter weights** and reuse **activations** **spatially** across the PE array
- Examples: [**Moons**, VLSI 2016], [**Thinker**, VLSI 2017]

Input Stationary (IS)

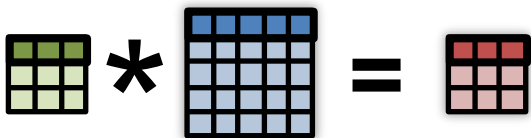


- **Minimize activation** read energy consumption
 - maximize convolutional and fmap reuse of activations
- **Unicast weights** and **accumulate partial sums** spatially across the PE array
- Example: [**SCNN**, ISCA 2017]

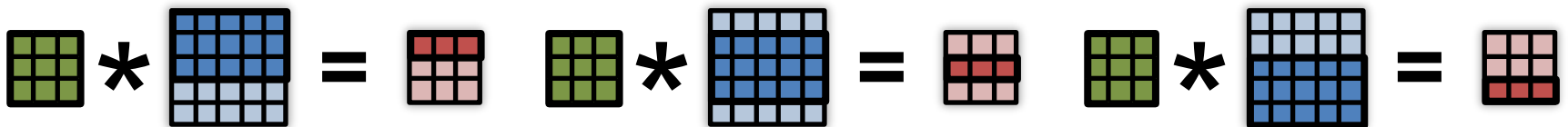
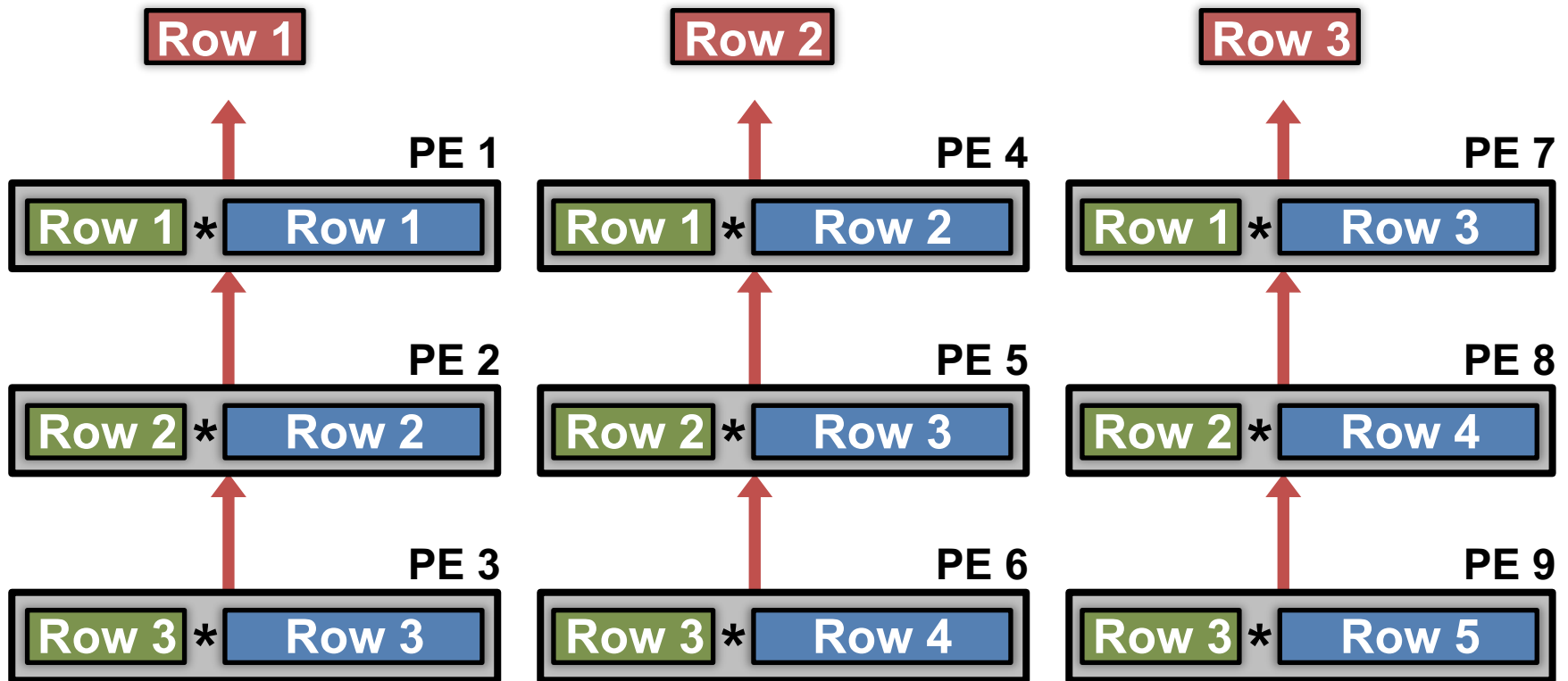
Row Stationary Dataflow



- Maximize row **convolutional reuse** in RF
 - Keep a **filter** row and **fmap** sliding window in RF
- Maximize row **psum accumulation** in RF

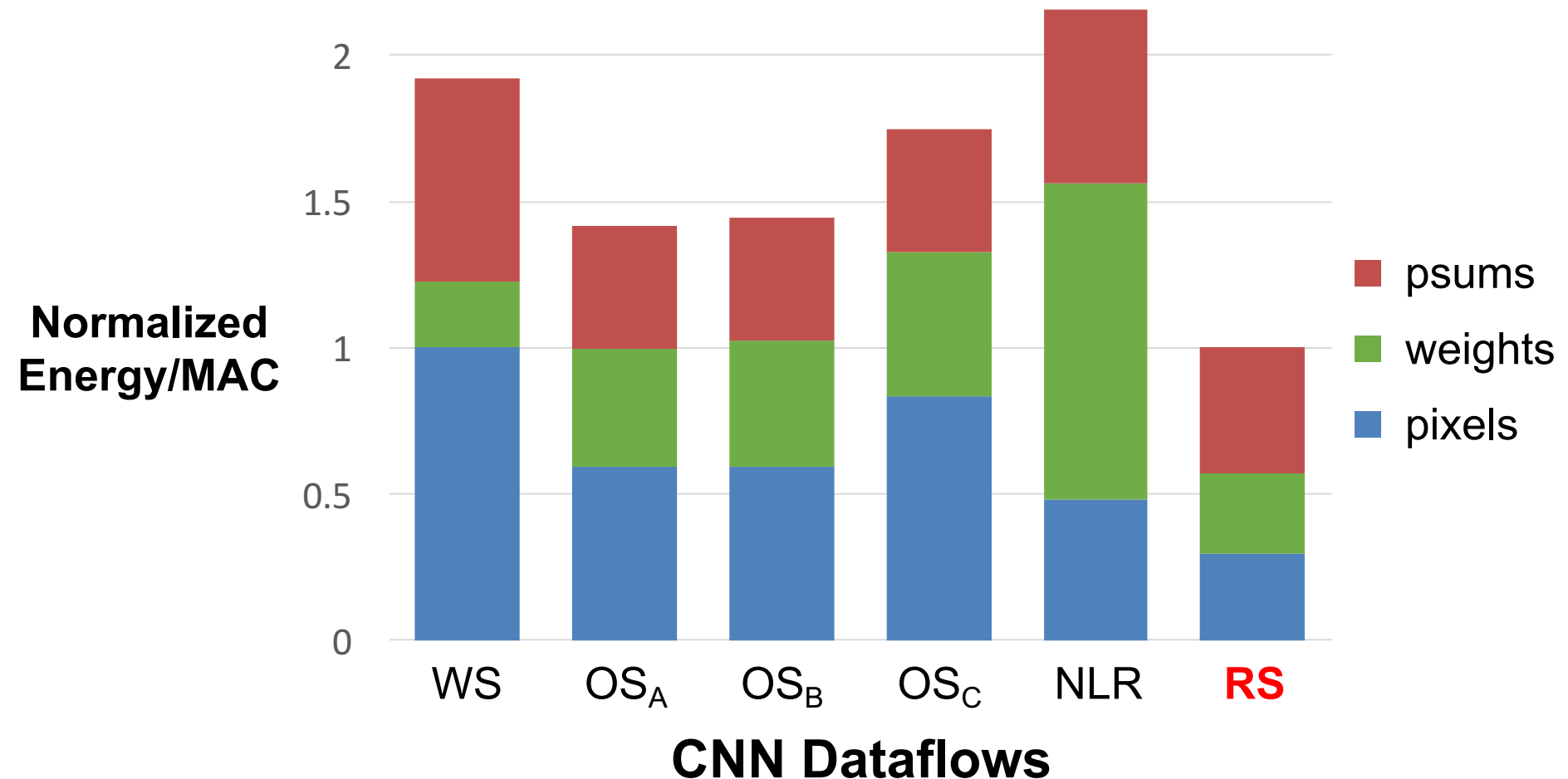


Row Stationary Dataflow



Optimize for **overall energy efficiency** instead
for only a certain data type

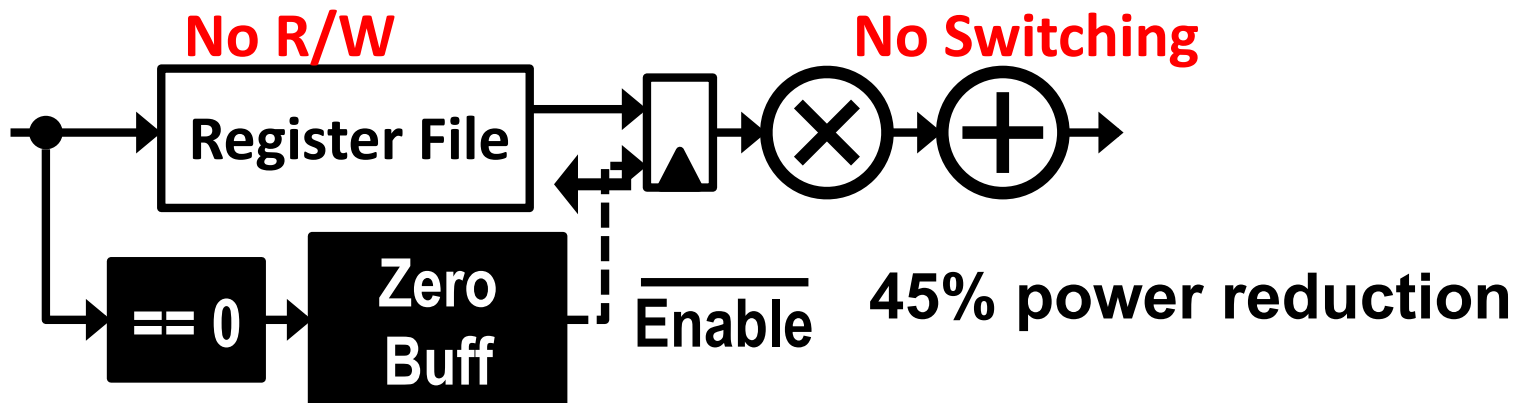
Dataflow Comparison: CONV Layers



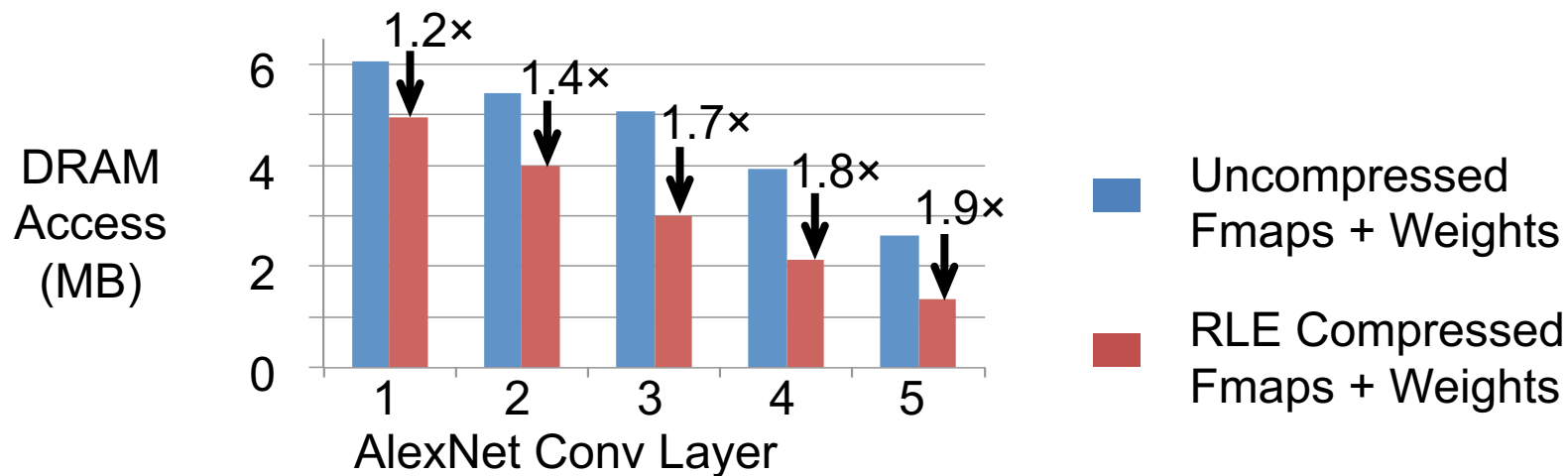
RS optimizes for the best **overall** energy efficiency

Exploit Sparsity

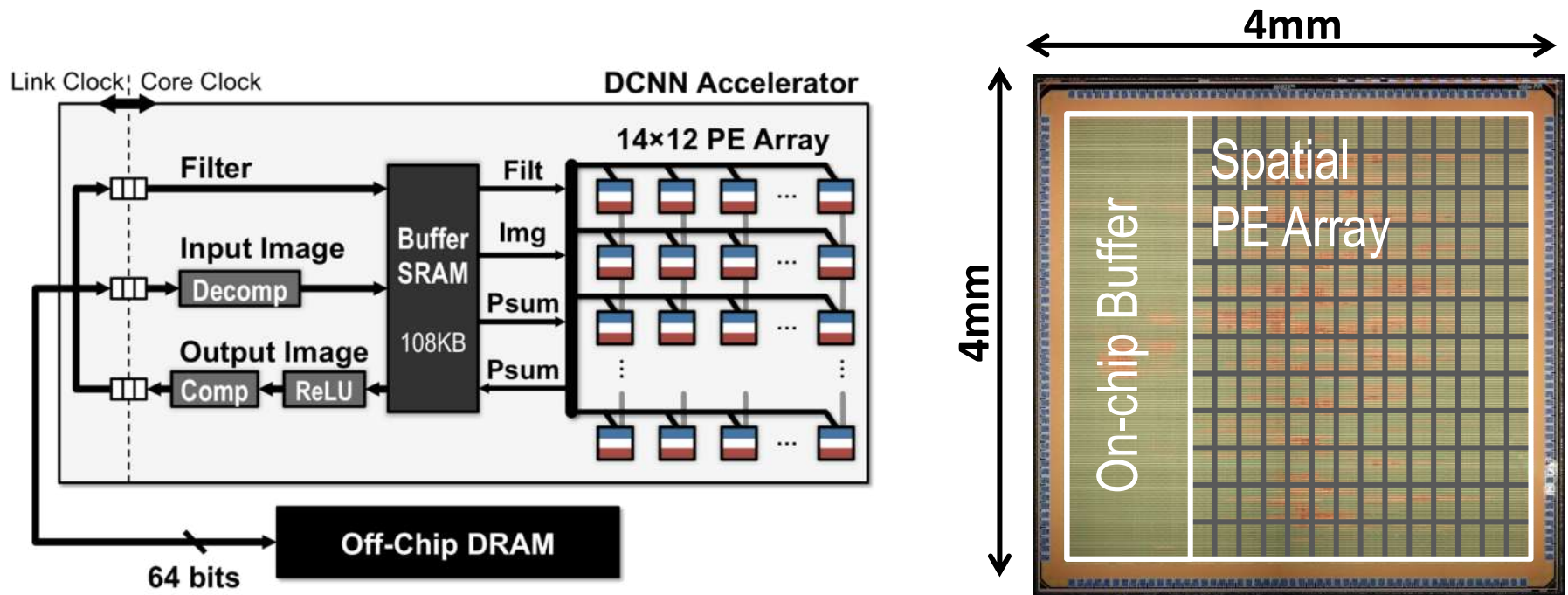
Method 1. Skip memory access and computation



Method 2. Compress data to reduce storage and data movement



Eyeriss: Deep Neural Network Accelerator



[Chen, ISSCC 2016]

*Exploits data reuse for **100x** reduction in memory accesses from global buffer and **1400x** reduction in memory accesses from off-chip DRAM*

Overall >10x energy reduction compared to a mobile GPU (Nvidia TK1)

Eyeriss Project Website: <http://eyeriss.mit.edu>

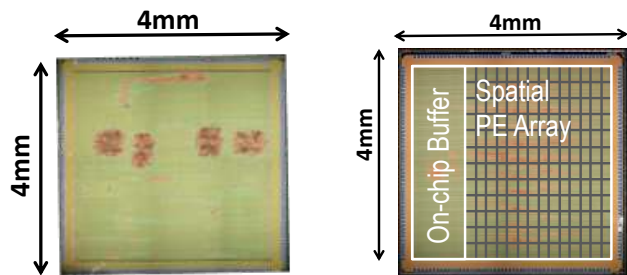
Results for AlexNet

Features: Energy vs. Accuracy

Exponential

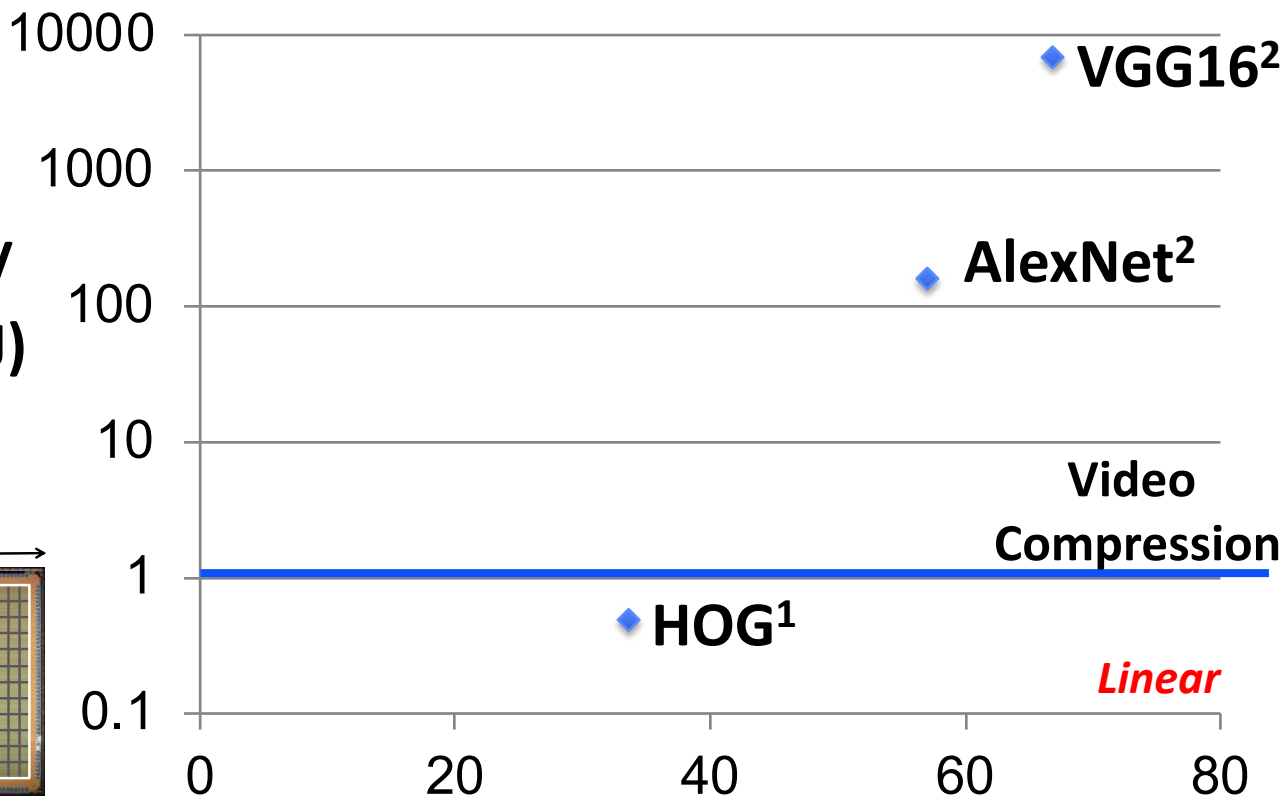
Energy/
Pixel (nJ)

*Measured in 65nm**



① [Suleiman, VLSI 2016] ② [Chen, ISSCC 2016]

** Only feature extraction. Does not include data, classification energy, augmentation and ensemble, etc.*



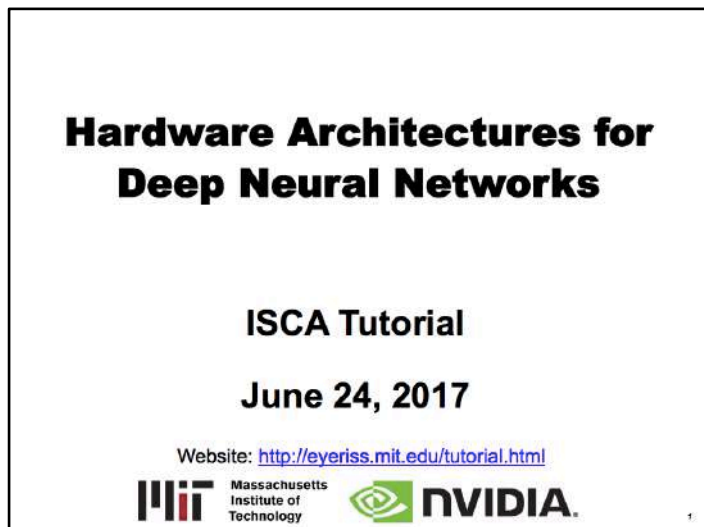
Accuracy (Average Precision)

Measured in on VOC 2007 Dataset

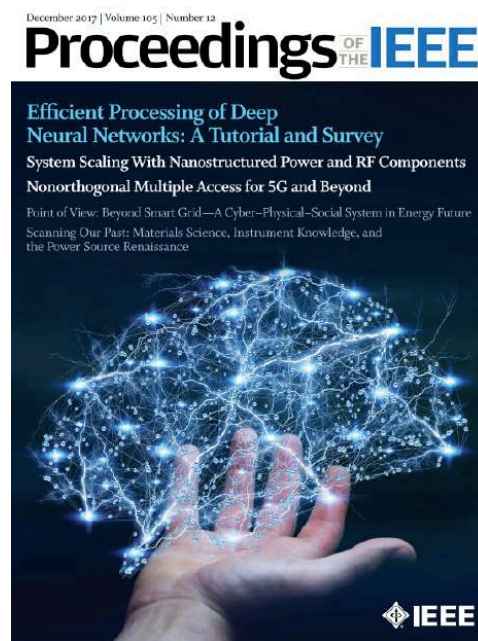
1. DPM v5 [Girshick, 2012]
2. Fast R-CNN [Girshick, CVPR 2015]

Energy-Efficient Processing of DNNs

A significant amount of algorithm and hardware research on energy-efficient processing of DNNs



<http://eyeriss.mit.edu/tutorial.html>



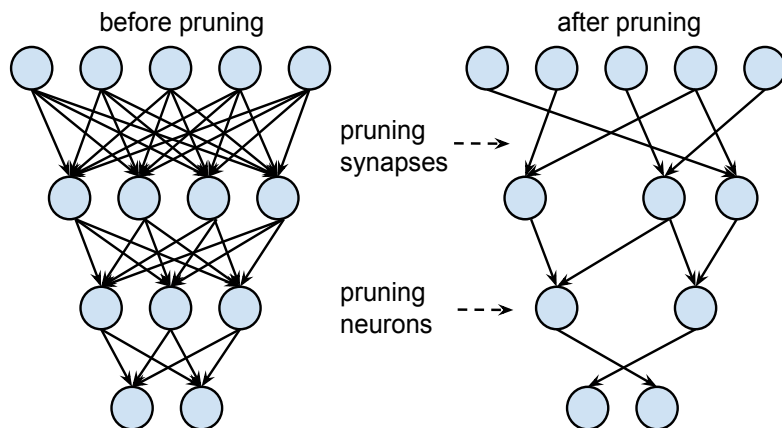
V. Sze, Y.-H. Chen,
T.-J. Yang, J. Emer,
*"Efficient Processing of
Deep Neural Networks:
A Tutorial and Survey,"*
Proceedings of the IEEE,
Dec. 2017

We identified various limitations to existing approaches

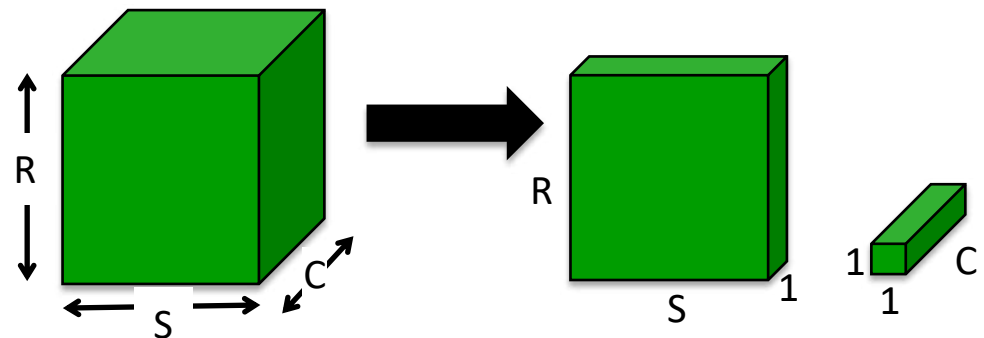
Design of Efficient DNN Algorithms

- Popular efficient DNN algorithm approaches

Network Pruning



Compact Network Architectures

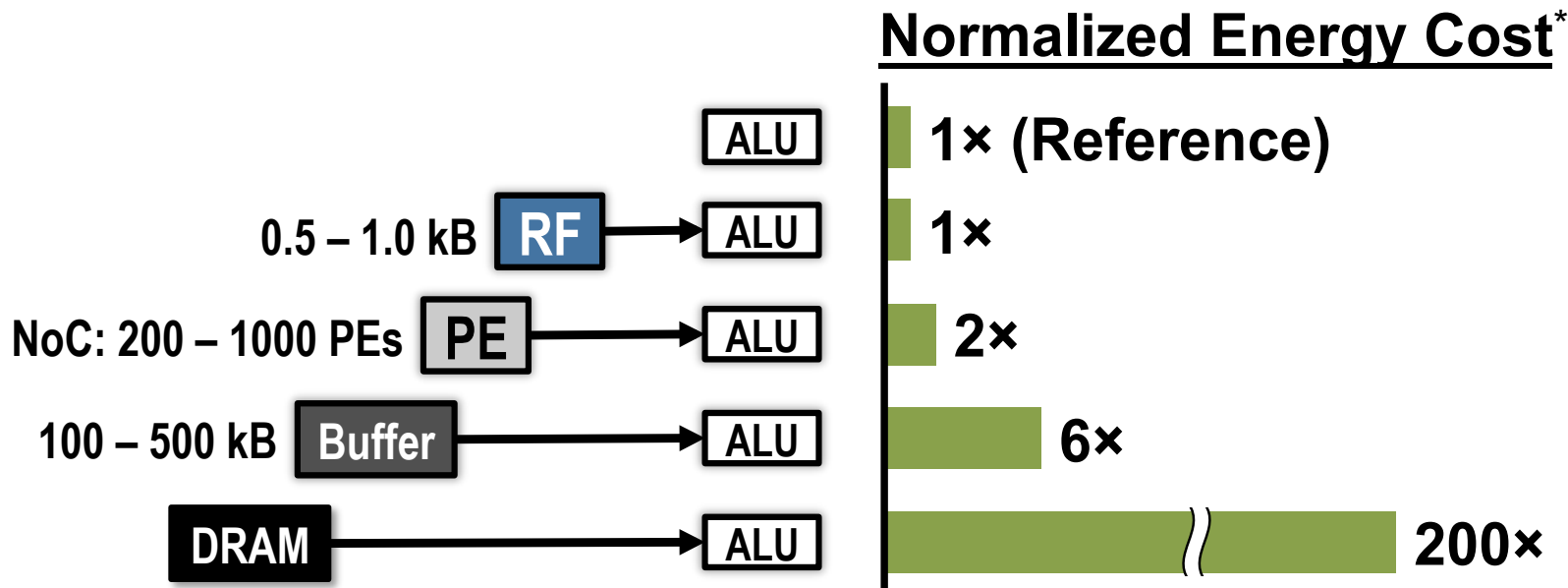
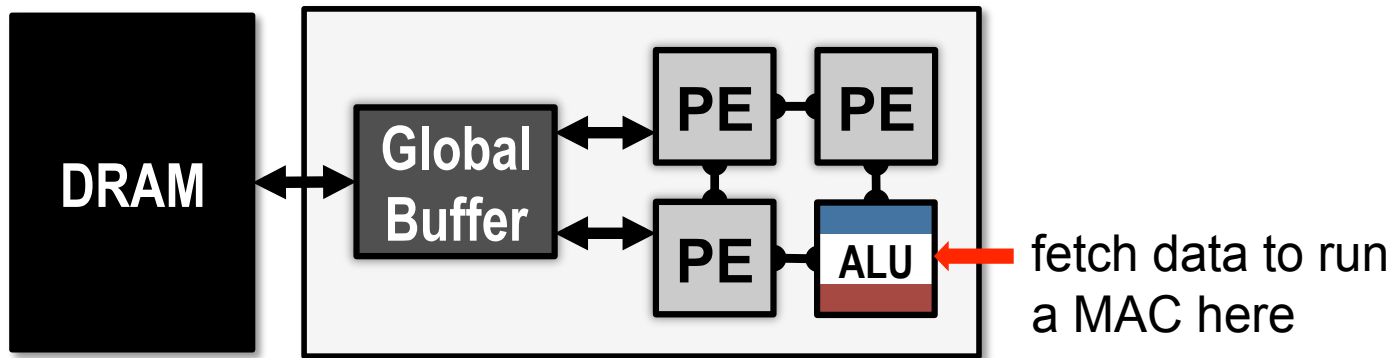


Examples: SqueezeNet, MobileNet

... also reduced precision

- Focus on reducing number of MACs and weights
- **Does it translate to energy savings and reduced latency?**

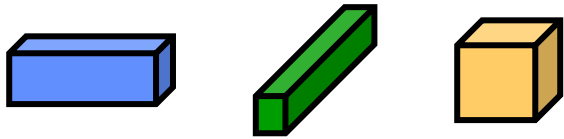
Data Movement is Expensive



* measured from a commercial 65nm process

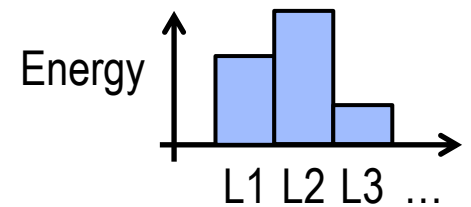
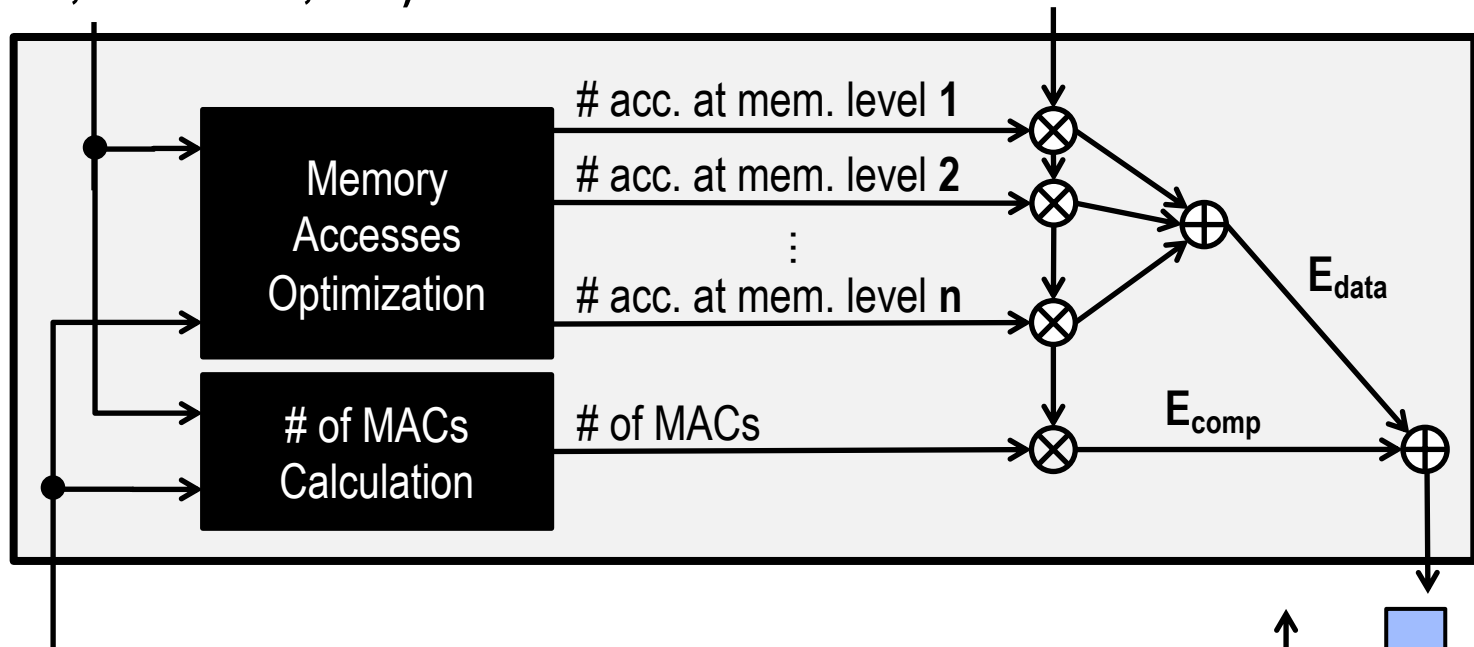
Energy of weight depends on **memory hierarchy** and **dataflow**

Energy-Evaluation Methodology



DNN Shape Configuration
(# of channels, # of filters, etc.)

**Hardware Energy Costs of each
MAC and Memory Access**



DNN Energy Consumption

DNN Weights and Input Data

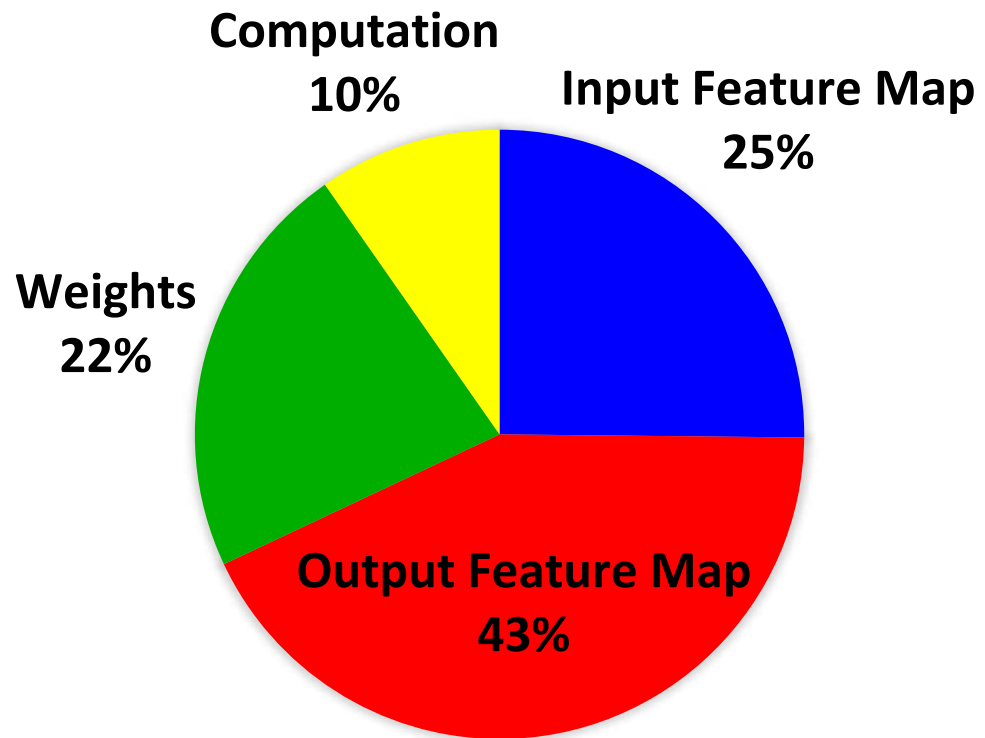
[0.3, 0, -0.4, 0.7, 0, 0, 0.1, ...]

Tool available at: <https://energyestimation.mit.edu/>

Key Observations

- Number of weights ***alone*** is not a good metric for energy
- **All data types** should be considered

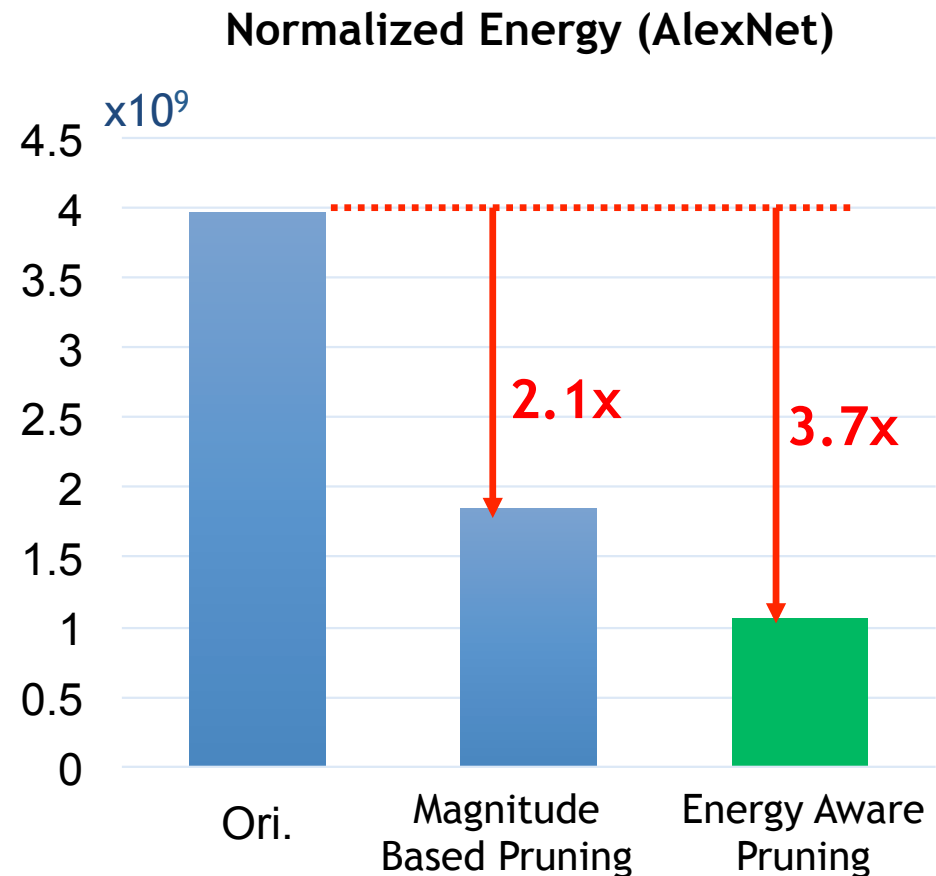
Energy Consumption of GoogLeNet



Energy-Aware Pruning

Directly target energy and incorporate it into the optimization of DNNs to provide greater energy savings

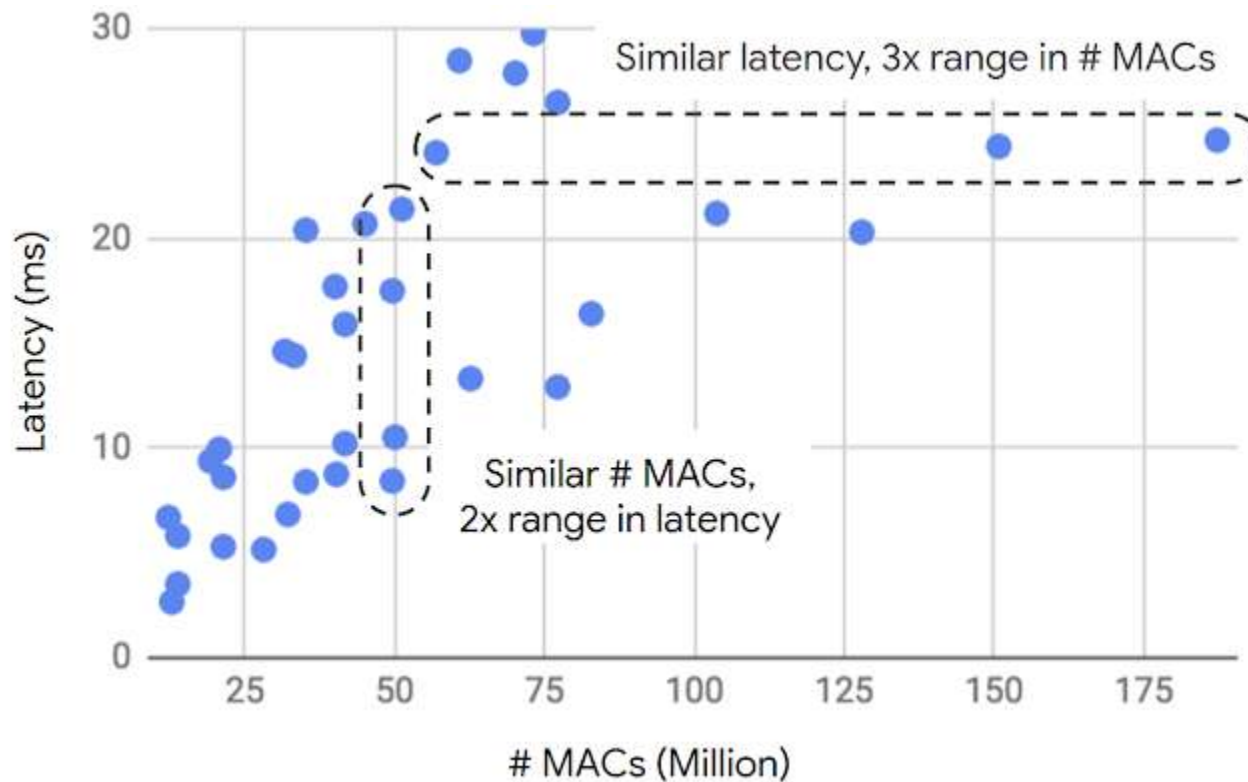
- Sort layers based on energy and prune layers that consume most energy first
- EAP reduces AlexNet energy by **3.7x** and outperforms the previous work that uses magnitude-based pruning by **1.7x**



Pruned models available at
<http://eyeriss.mit.edu/energy.html>

of Operations vs. Latency

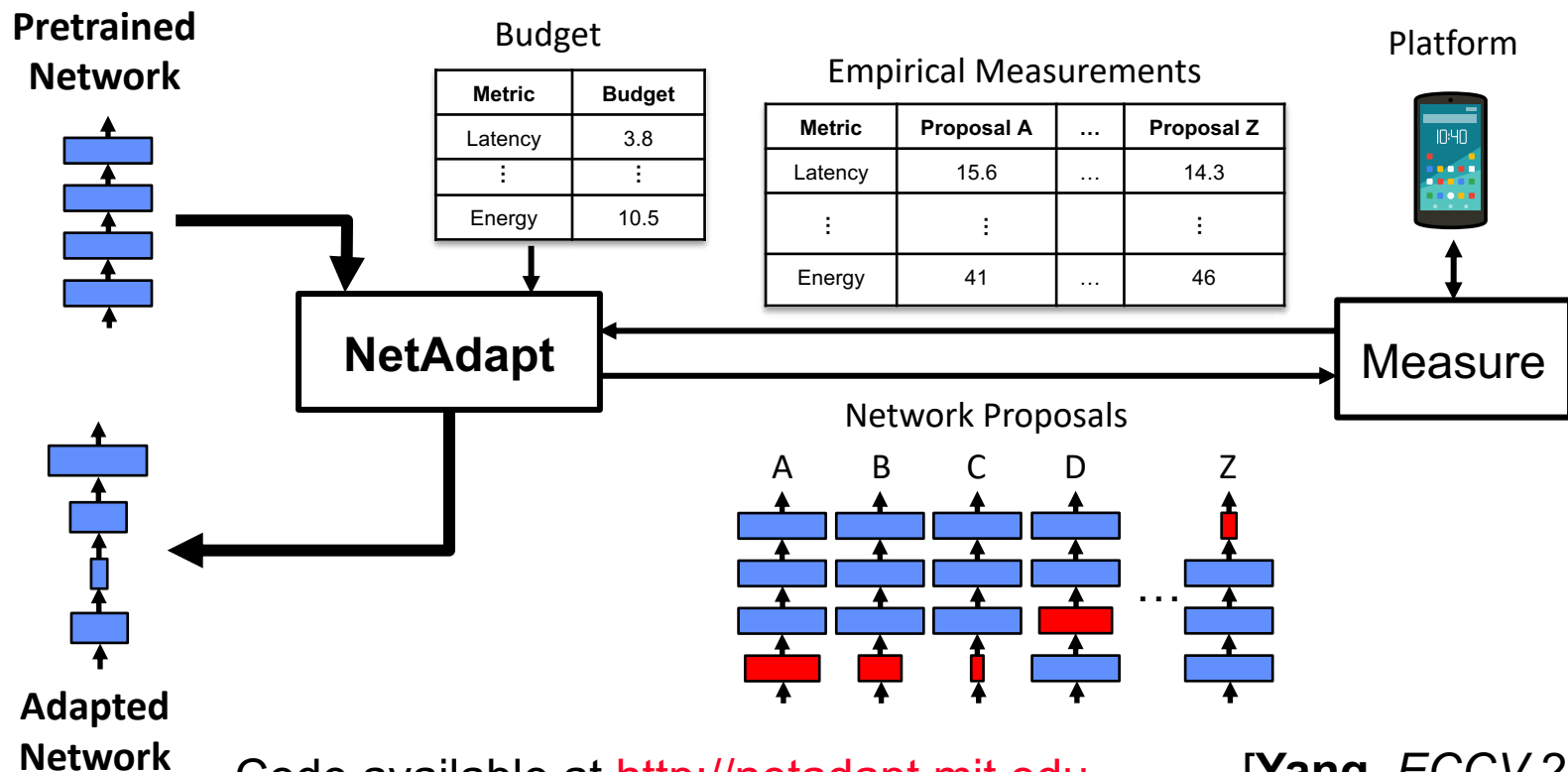
- # of operations (MACs) does not approximate latency well



Source: Google (<https://ai.googleblog.com/2018/04/introducing-cvpr-2018-on-device-visual.html>)

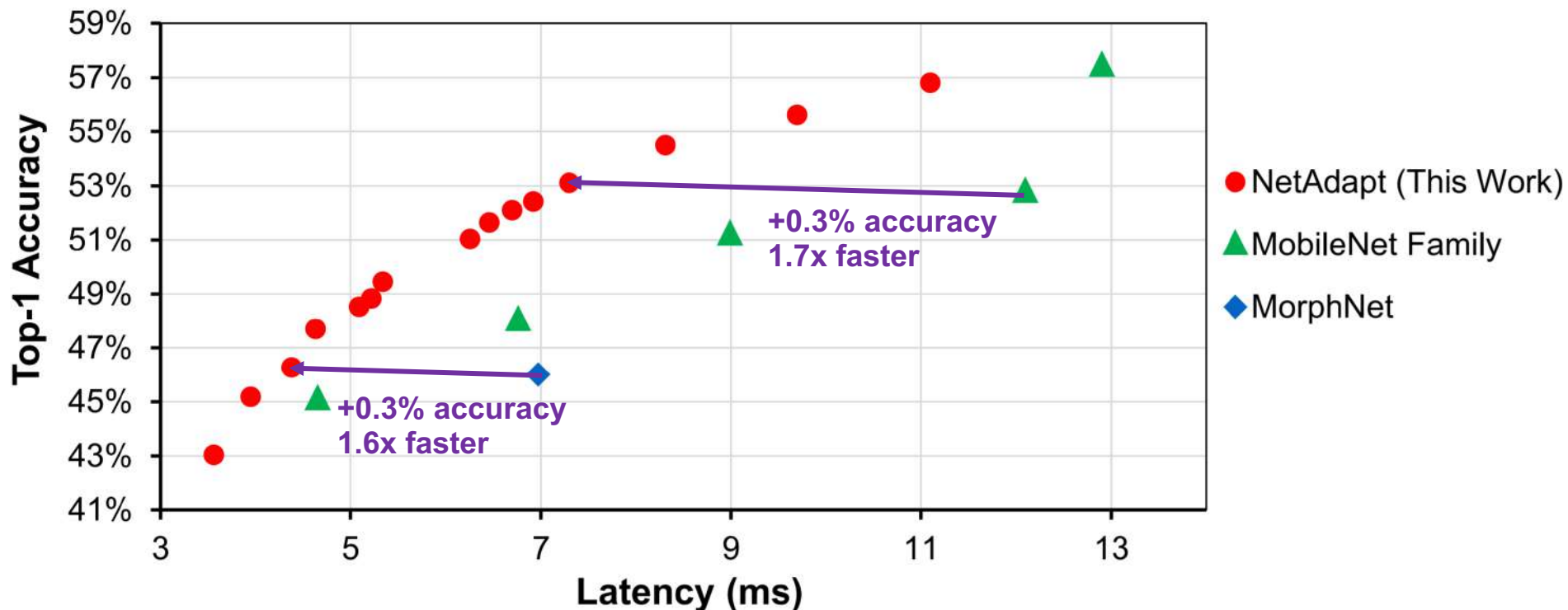
NetAdapt: Platform-Aware DNN Adaptation

- **Automatically adapt DNN** to a mobile platform to reach a target latency or energy budget
- Use **empirical measurements** to guide optimization (avoid modeling of tool chain or platform architecture)



Improved Latency vs. Accuracy Tradeoff

- NetAdapt boosts **the real inference speed** of MobileNet by up to 1.7x with higher accuracy



*Tested on the ImageNet dataset and a Google Pixel 1 CPU

Reference:

MobileNet: Howard et al, "Mobilenets: Efficient convolutional neural networks for mobile vision applications", arXiv 2017

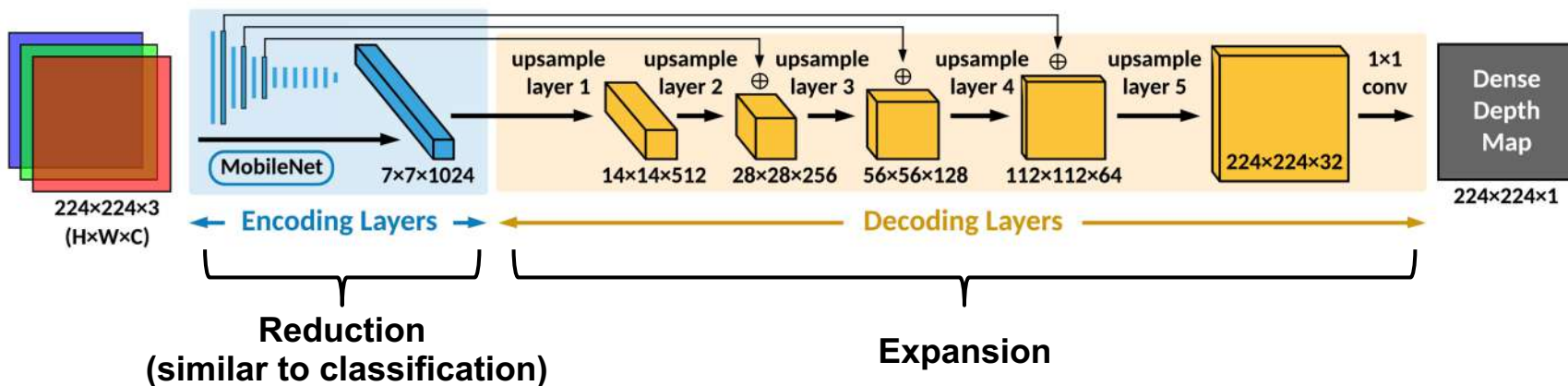
MorphNet: Gordon et al., "Morphnet: Fast & simple resource-constrained structure learning of deep networks", CVPR 2018

FastDepth: Fast Monocular Depth Estimation

Depth estimation from a single RGB image desirable, due to the relatively low cost and size of monocular cameras.

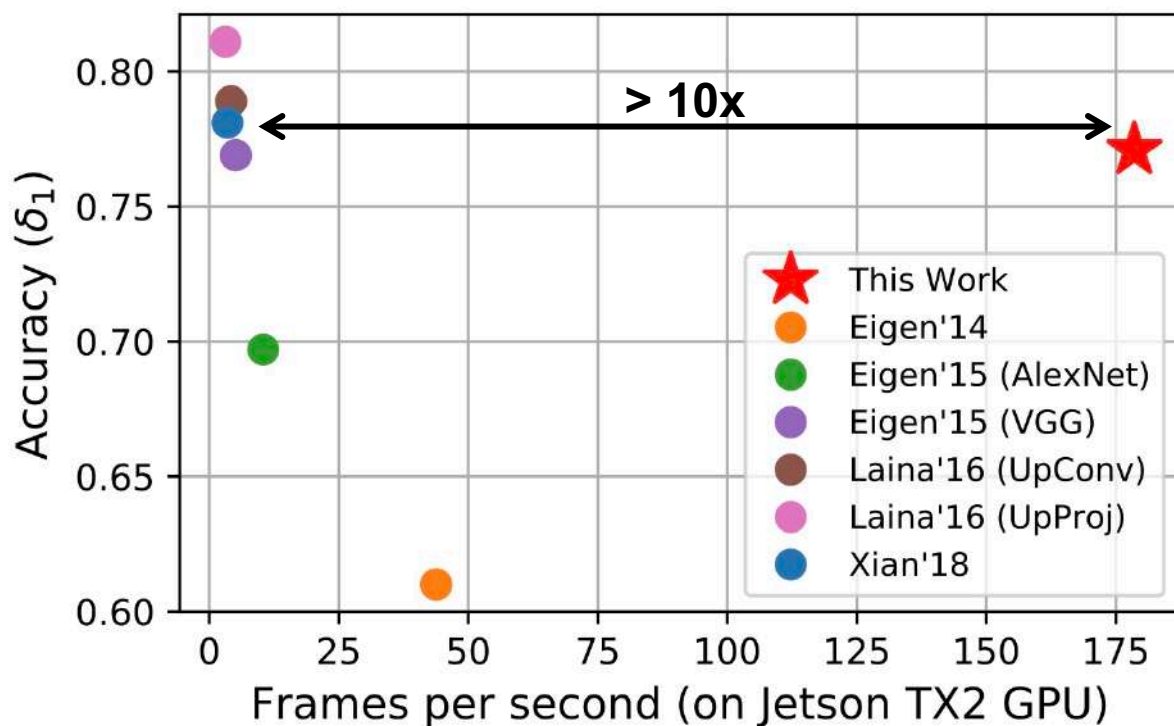


Auto Encoder DNN Architecture (Dense Output)



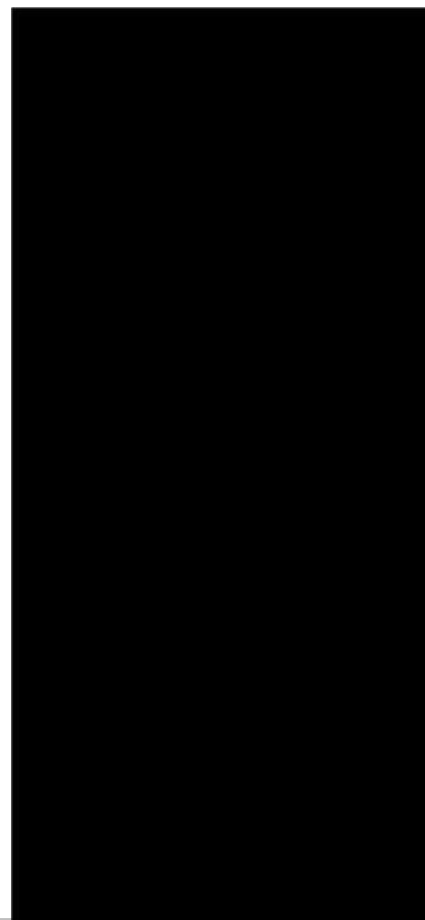
FastDepth: Fast Monocular Depth Estimation

Apply *NetAdapt*, *compact network design*, and *depth wise decomposition* to decoder layer to enable depth estimation at **high frame rates on an embedded platform** while still maintaining accuracy



Configuration: Batch size of one (32-bit float)

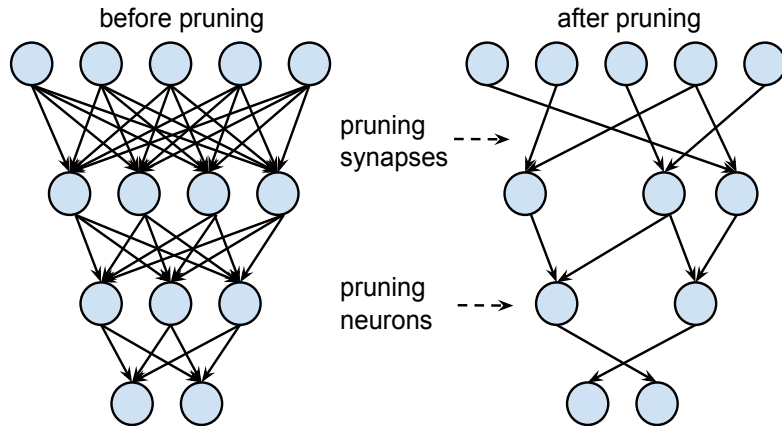
Models available at <http://fastdepth.mit.edu>



~40fps on
an iPhone

Many Efficient DNN Design Approaches

Network Pruning



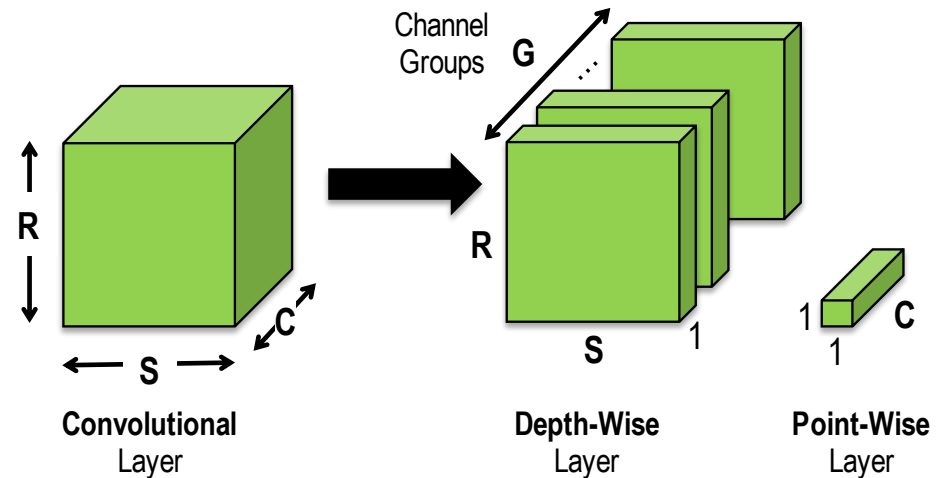
Reduce Precision

32-bit float 101010000000010100000000100

8-bit fixed 01100110

Binary 0

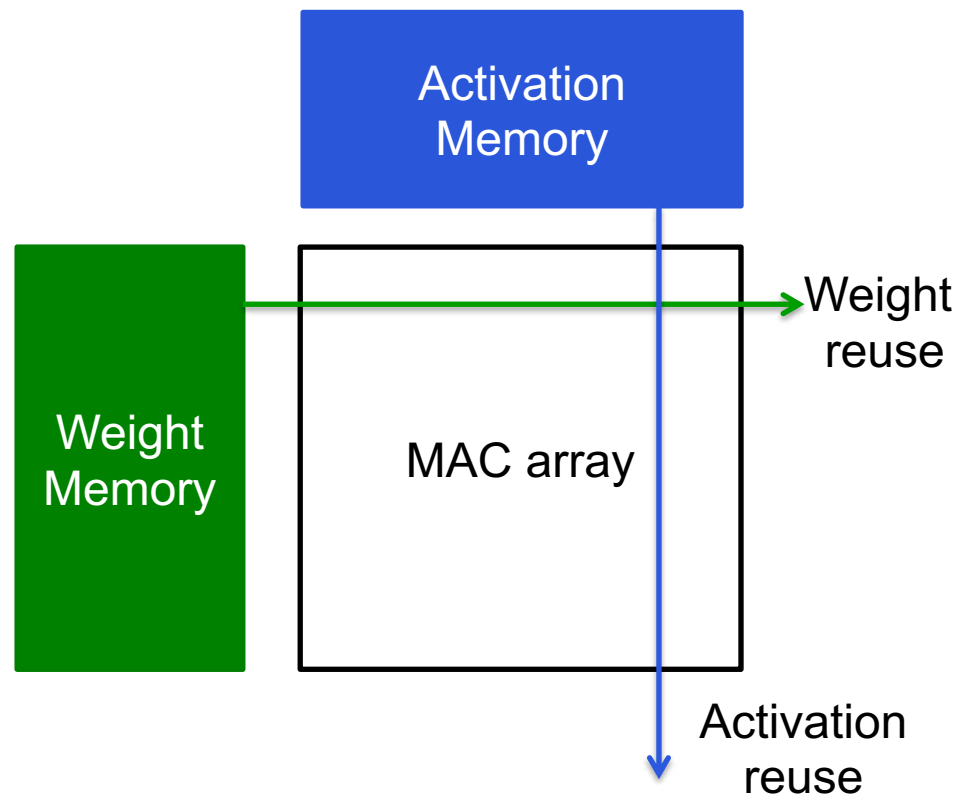
Compact Network Architectures



No guarantee that DNN algorithm designer will use a given approach.
Need flexible hardware!

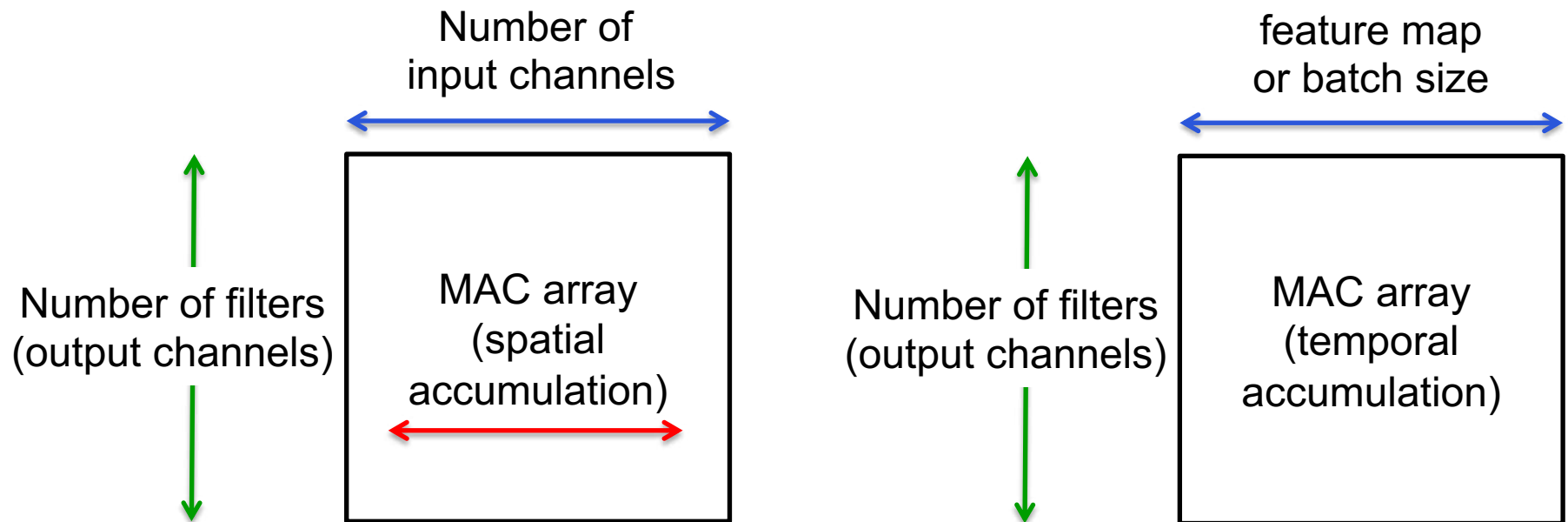
Existing DNN Architectures

- Specialized DNN hardware often rely on certain properties of DNN in order to achieve high energy-efficiency
- Example:** Reduce memory access by amortizing across MAC array



Limitation of Existing DNN Architectures

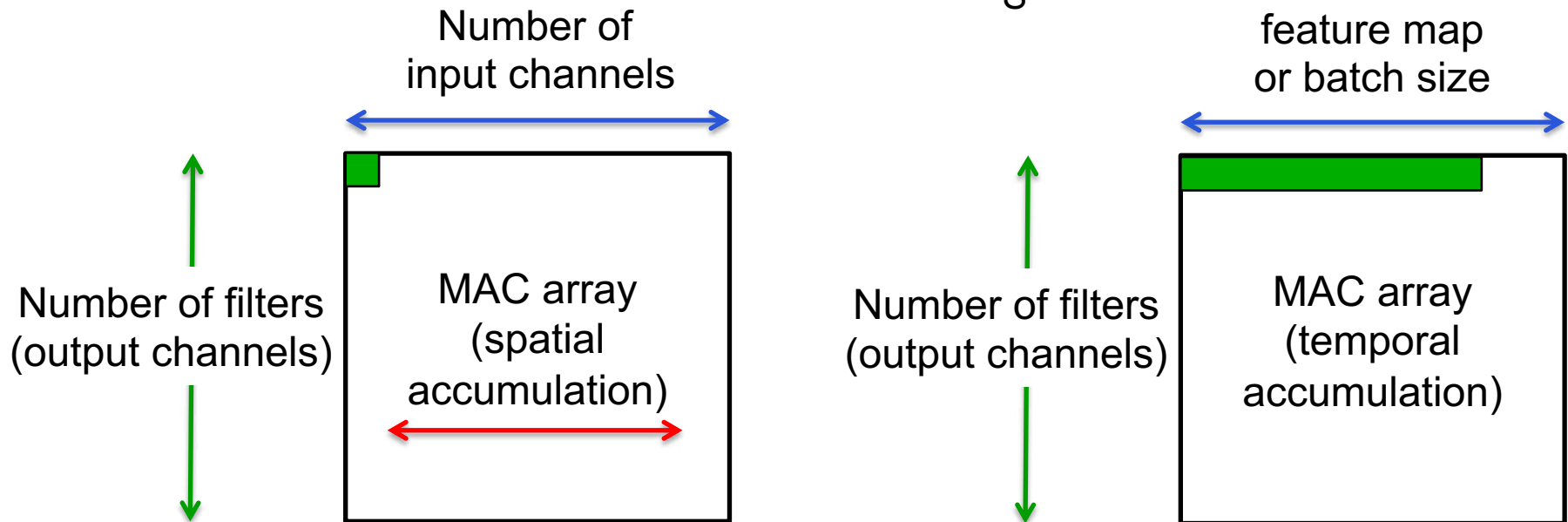
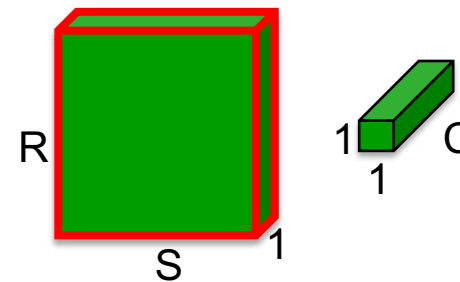
- **Example:** Reuse and array utilization depends on # of channels, feature map/batch size
 - Not efficient across all network architectures (e.g., compact DNNs)



Limitation of Existing DNN Architectures

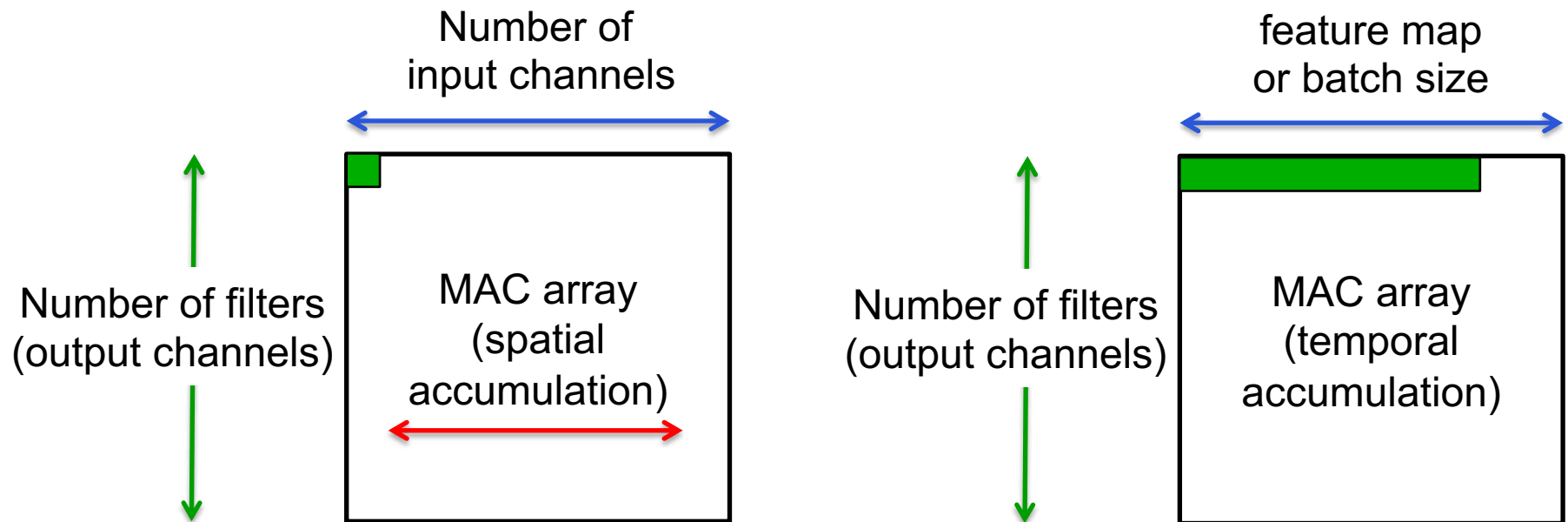
- **Example:** Reuse and array utilization depends on # of channels, feature map/batch size
 - Not efficient across all network architectures (e.g., compact DNNs)

Example mapping for
depth wise layer



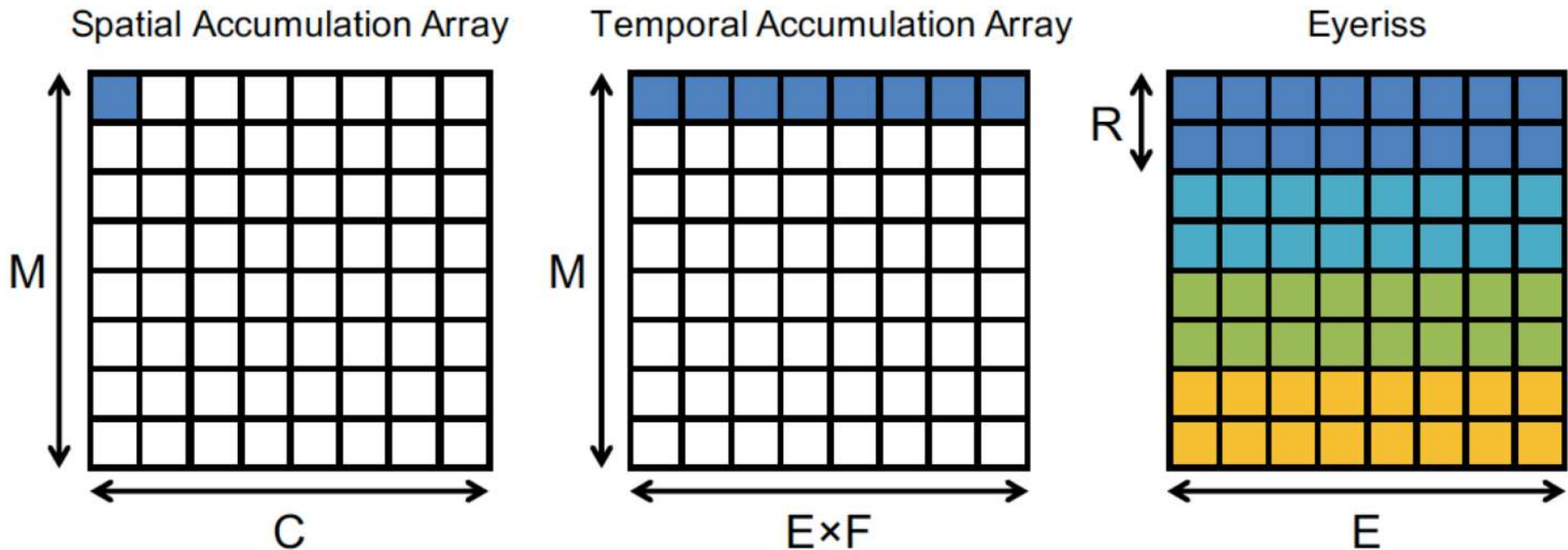
Limitation of Existing DNN Architectures

- **Example:** Reuse and array utilization depends on # of channels, feature map/batch size
 - Not efficient across all network architectures (e.g., compact DNNs)
 - Less efficient as array scales up in size
 - Can be challenging to exploit sparsity



Need Flexible Dataflow

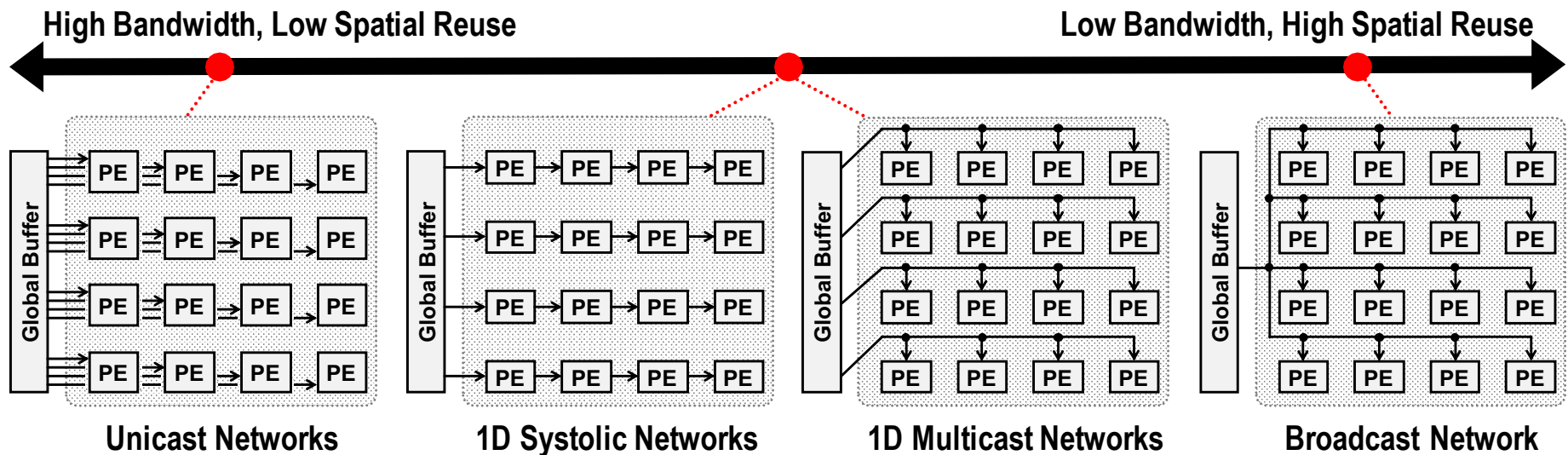
- Use flexible dataflow (**Row Stationary**) to exploit reuse in any dimension of DNN to increase energy efficiency and array utilization



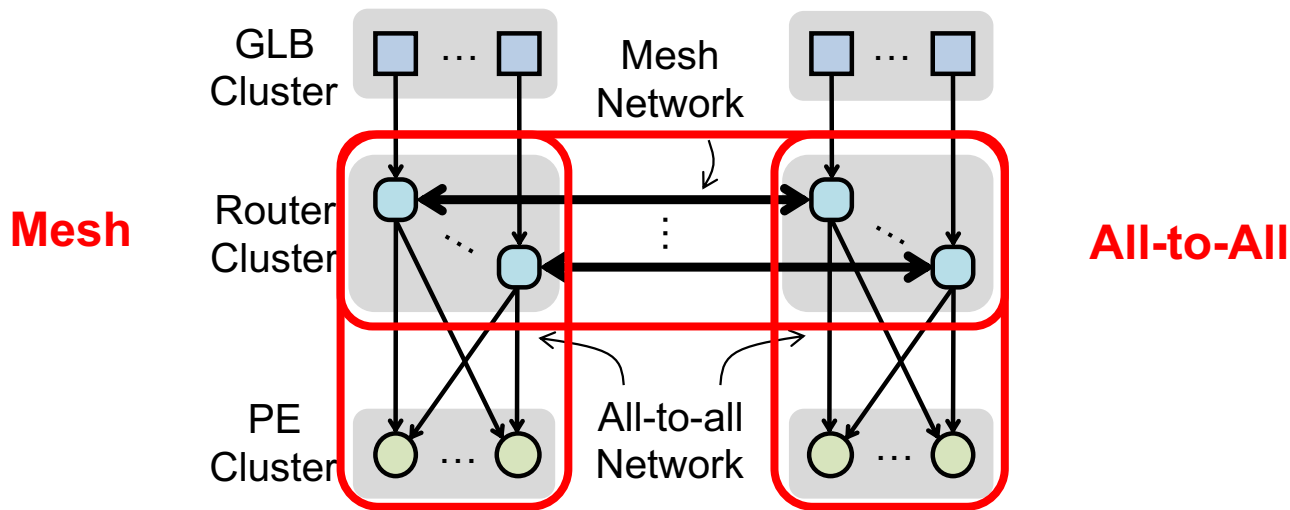
Example: Depth-wise layer

Need Flexible NoC for Varying Reuse

- When reuse available, need **multicast** to exploit spatial data reuse for energy efficiency and high array utilization
- When reuse not available, need **unicast** for high BW for weights for FC and weights & activations for high PE utilization
- An **all-to-all** satisfies above but too expensive and not scalable



Hierarchical Mesh

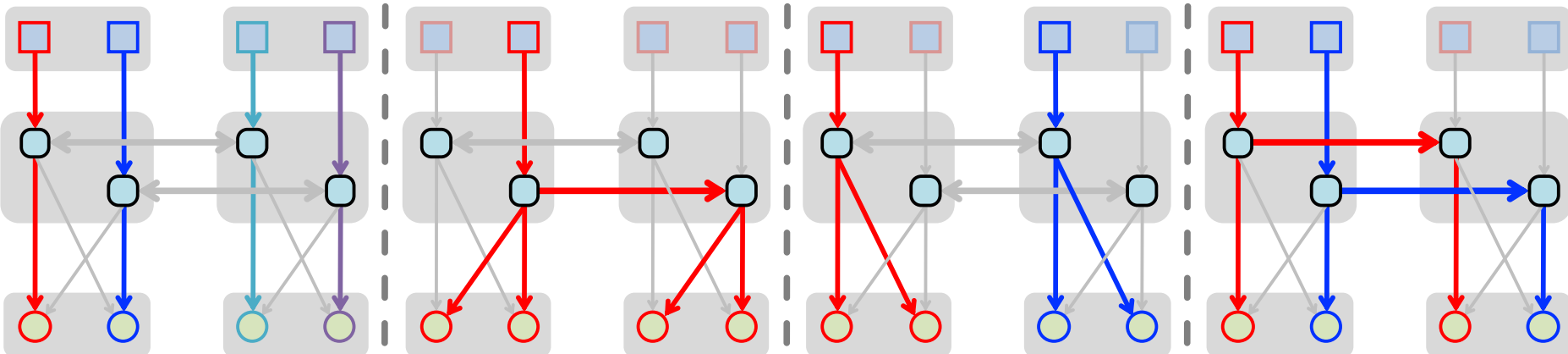


High Bandwidth

High Reuse

Grouped Multicast

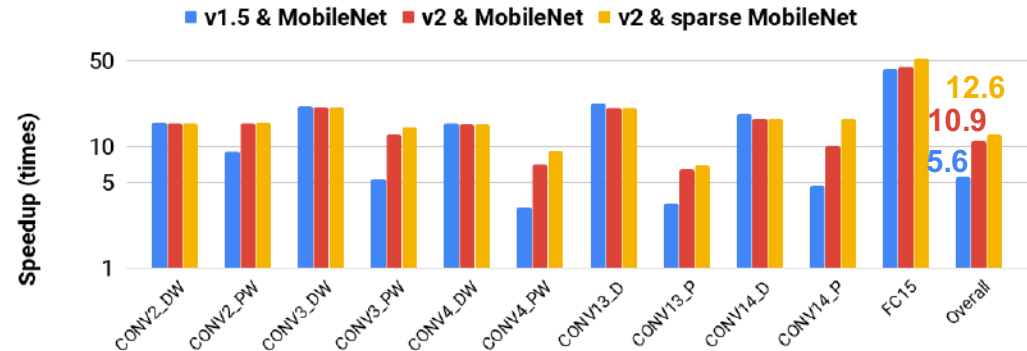
Interleaved Multicast



Eyeriss v2: Balancing Flexibility and Efficiency

Efficiently supports

- Wide range of filter shapes
 - Large **and** Compact
- Different Layers
 - **CONV, FC, depth wise, etc.**
- Wide range of sparsity
 - Dense **and** Sparse
- **Scalable architecture**



Speed up over Eyeriss v1 scales with number of PEs

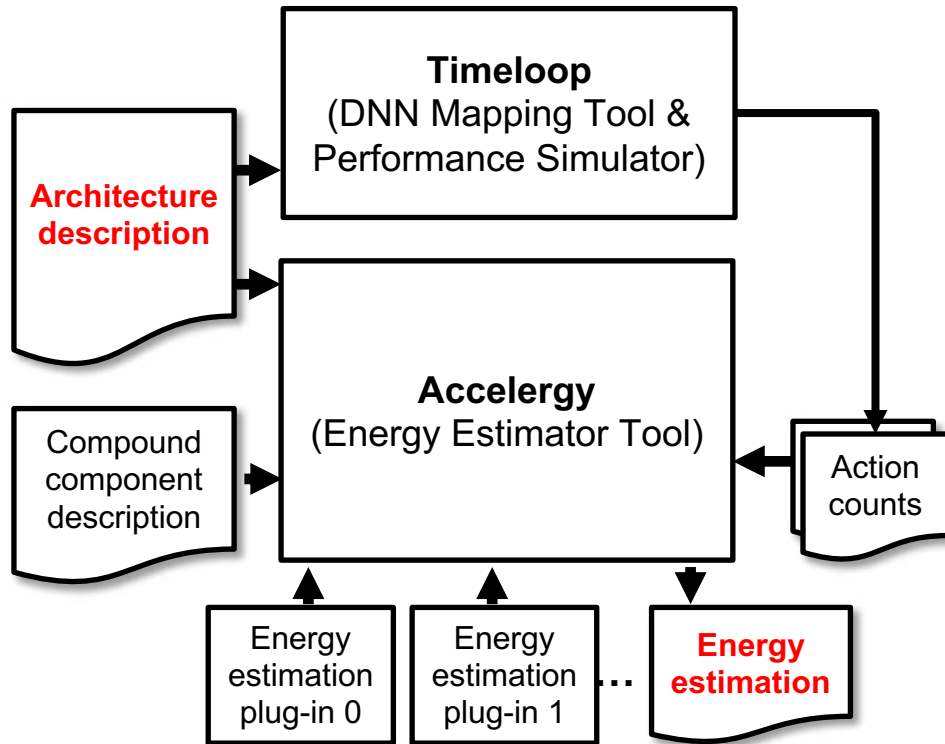
# of PEs	256	1024	16384
AlexNet	17.9x	71.5x	1086.7x
GoogLeNet	10.4x	37.8x	448.8x
MobileNet	15.7x	57.9x	873.0x

Over an order of magnitude faster and more energy efficient than Eyeriss v1

[Chen, JETCAS 2019]

DL Processor Evaluation Tools

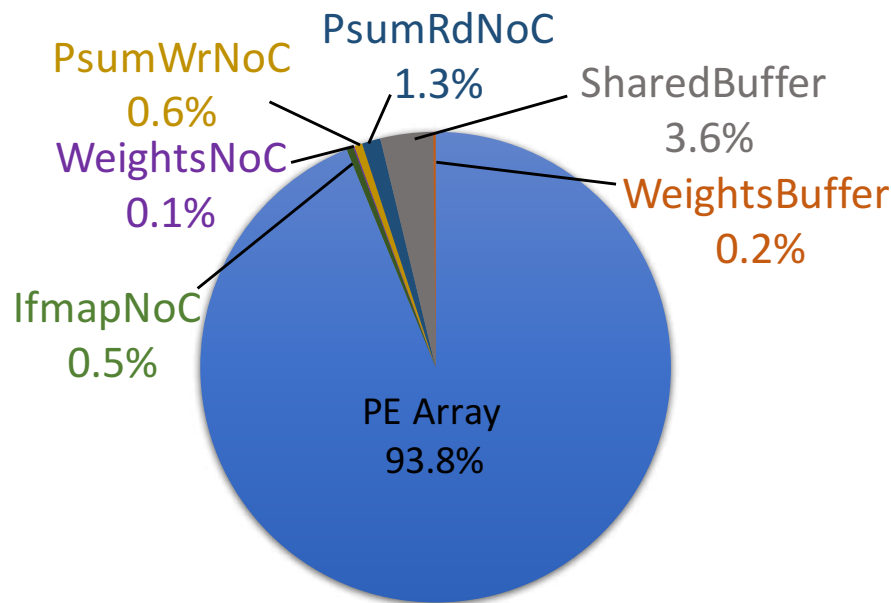
- Require systematic way to
 - Evaluate and compare wide range of DL processor designs
 - Rapidly explore design space
- **Accelergy** [Wu, ICCAD 2019]
 - Early stage energy estimation tool at the architecture level
 - Estimate energy consumption based on architecture level components (e.g., # of PEs, GLB size, NoC)
 - Evaluate architecture level energy impact of emerging devices
 - Plug-ins for different technologies
- **Timeloop** [Parashar, ISPASS 2019]
 - DNN mapping tool
 - Performance Simulator → Action counts



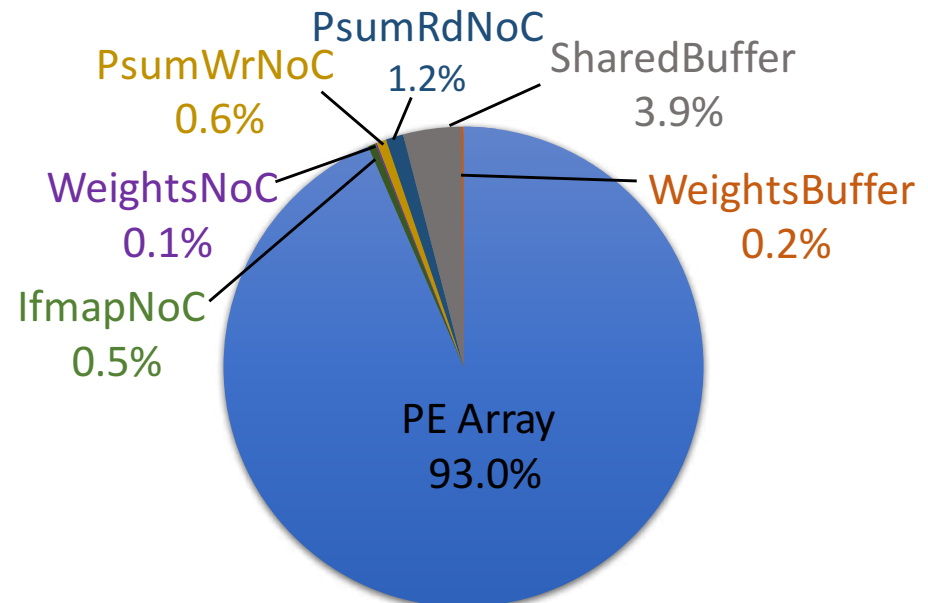
Open-source code available at:
<http://accelergy.mit.edu>

Accelergy Estimation Validation

- Validation on Eyeriss [Chen, ISSCC 2016]
 - Achieves 95% accuracy compared to post-layout simulations
 - Can accurately captures energy breakdown at different granularities



Ground Truth Energy Breakdown



Accelergy Energy Breakdown

Open-source code available at: <http://accelergy.mit.edu>

[Wu, ICCAD 2019]

Visual-Inertial Localization

Determines location/orientation of robot from images and IMU

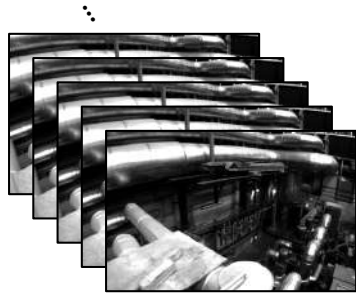
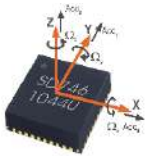


Image sequence

IMU

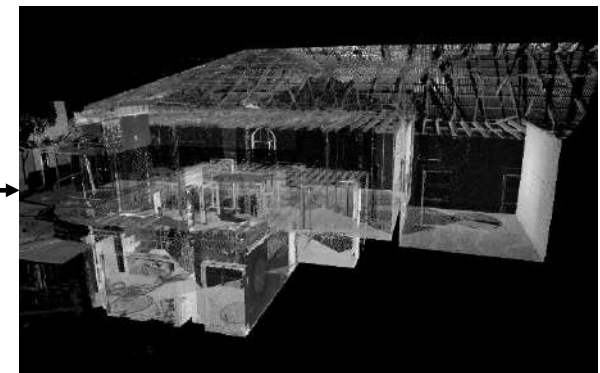
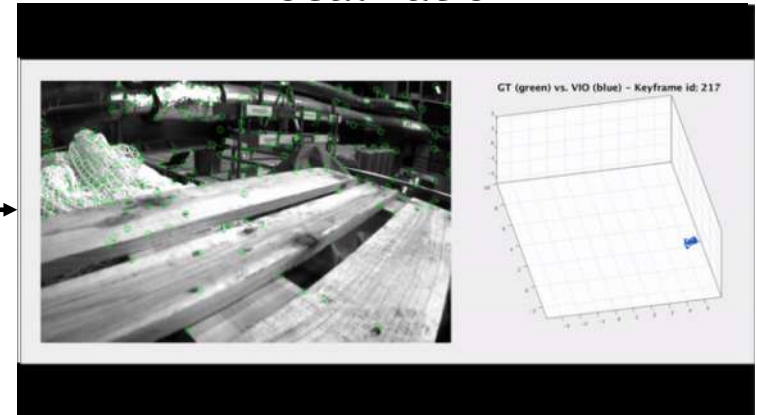
Inertial Measurement Unit



Visual-Inertial
Odometry
(VIO)*

*Subset of SLAM algorithm
(Simultaneous Localization And Mapping)

Localization



Mapping

Localization at Under 25 mW

First chip that performs **complete** Visual-Inertial Odometry

Front-End for camera

(Feature detection, tracking, and outlier elimination)

Front-End for IMU

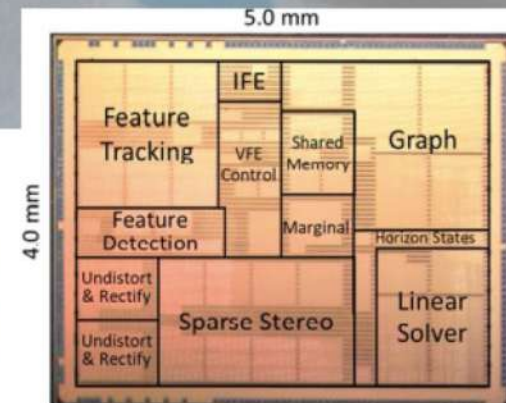
(pre-integration of accelerometer and gyroscope data)

Back-End Optimization of Pose Graph

Consumes **684×** and **1582×** less energy than mobile and desktop CPUs, respectively



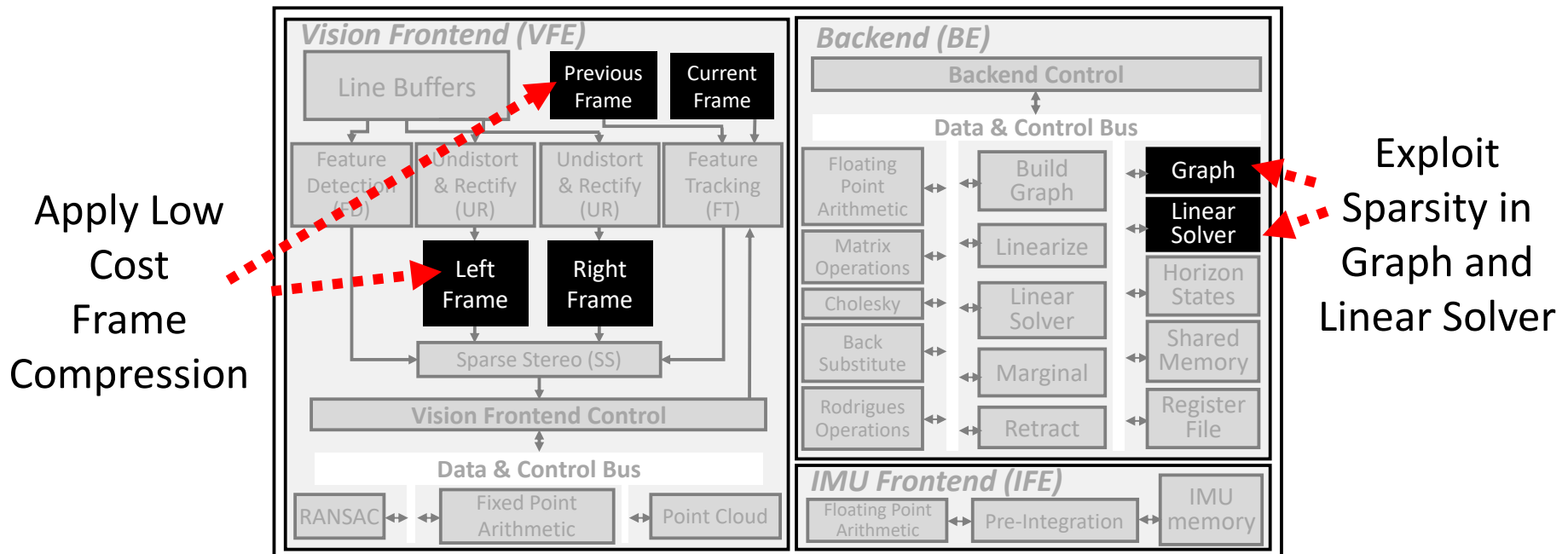
Technology	65nm CMOS	Supply	1 V
Chip area (mm ²)	4.0 x 5.0	Resolution	752x480
Core area (mm ²)	3.54 x 4.54	Camera rate	28 - 171 fps
Logic gates	2,043 kgates	Keyframe rate	16 - 90 fps
SRAM	854KB	Average Power	24 mW
VFE Frequency	62.5 MHz	GOPS	10.5 - 59.1
BE Frequency	83.3 MHz	GFLOPS	1 - 5.7



[Zhang*, Suleiman*, RSS 2017], [Suleiman, VLSI 2018]

Key Methods to Reduce Data Size

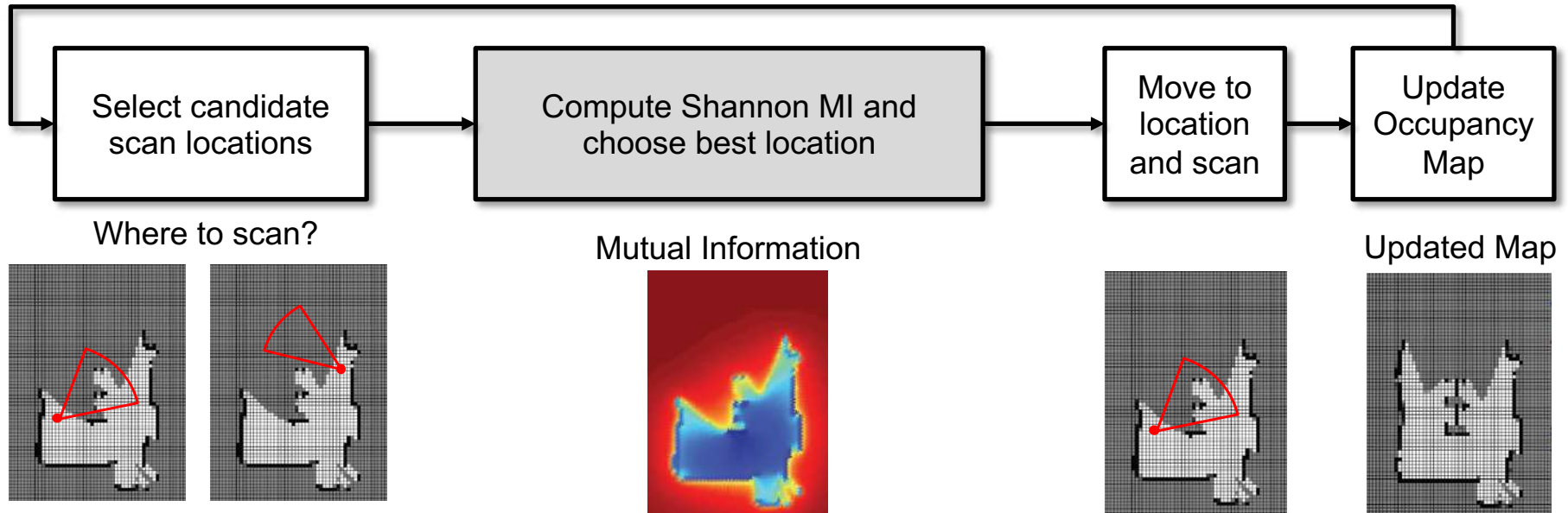
Navion: Fully integrated system – no off-chip processing or storage



Use **compression** and **exploit sparsity** to reduce memory down to 854kB

Where to Go Next: Planning and Mapping

Robot Exploration: Decide where to go by computing Shannon Mutual Information



Exploration with a mini race car using motion capture for localization

[Zhang, ICRA 2019]

Vivienne Sze ([@eems_mit](#))

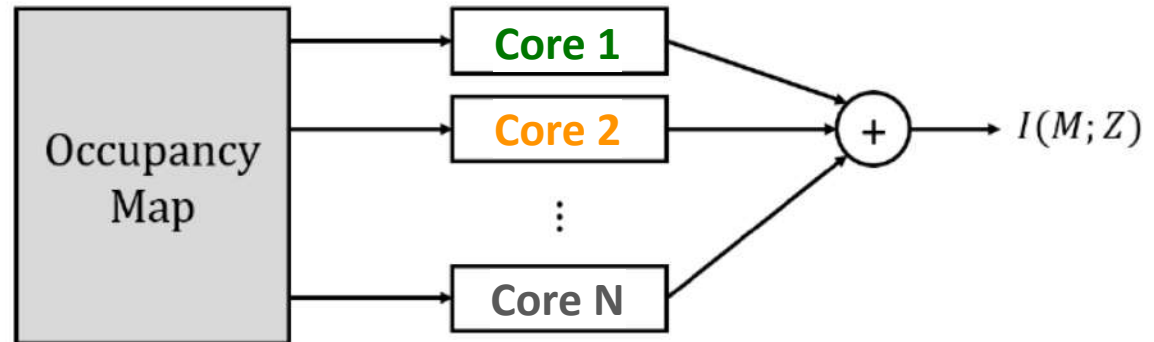
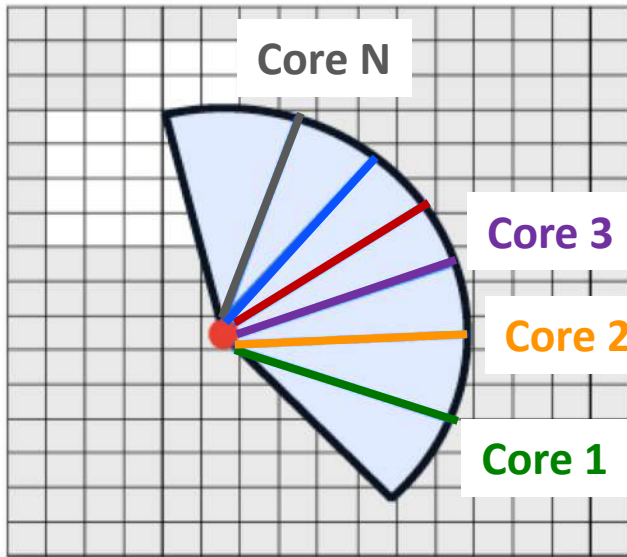


Occupancy map with planned path

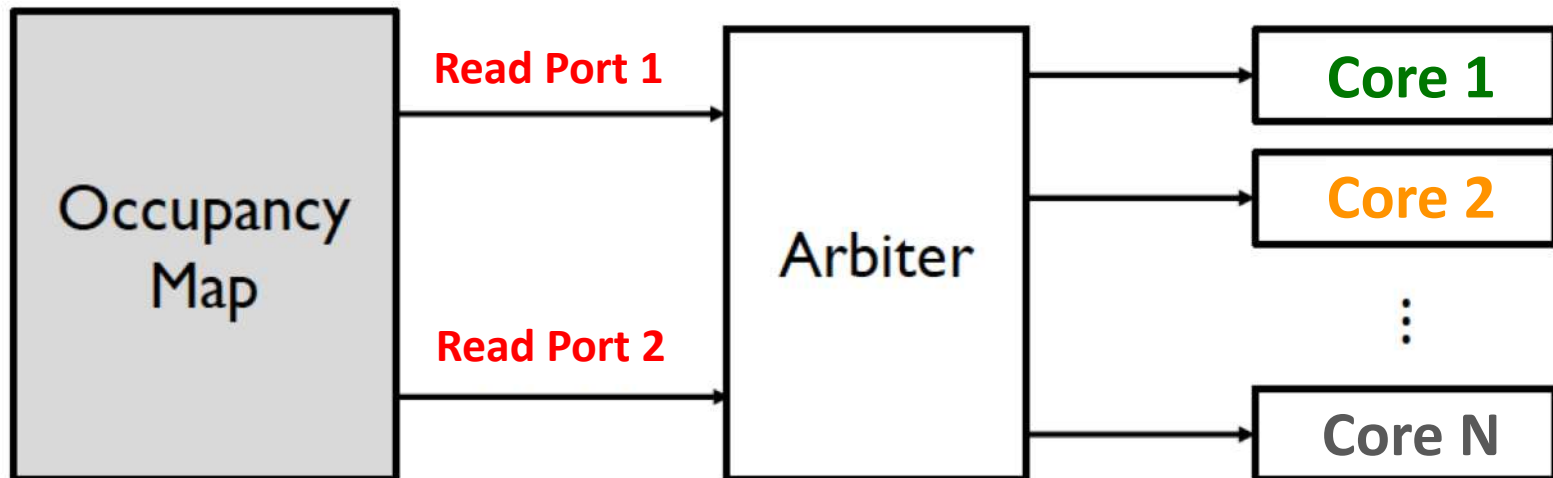
MI surface

Challenge is Data Delivery to All Cores

Process multiple beams in parallel



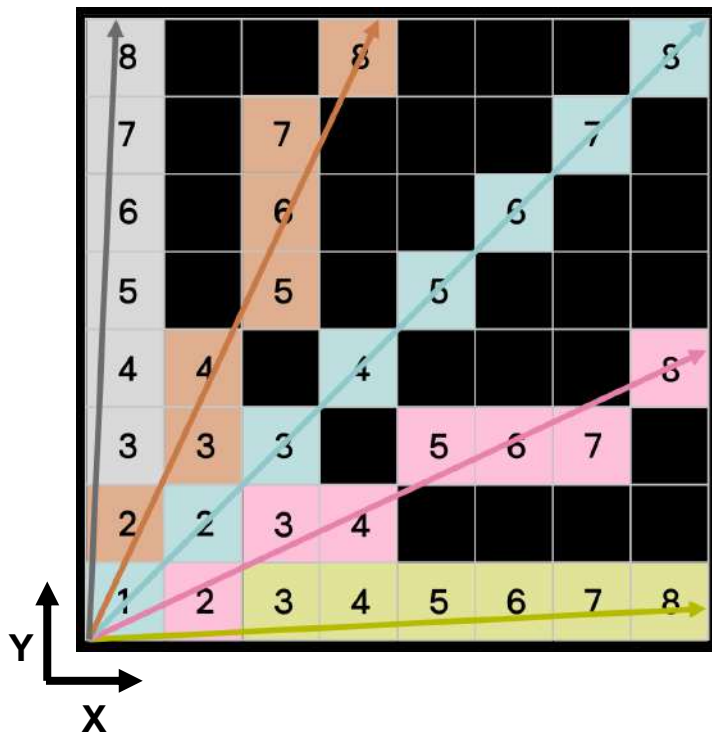
Data delivery from memory is limited



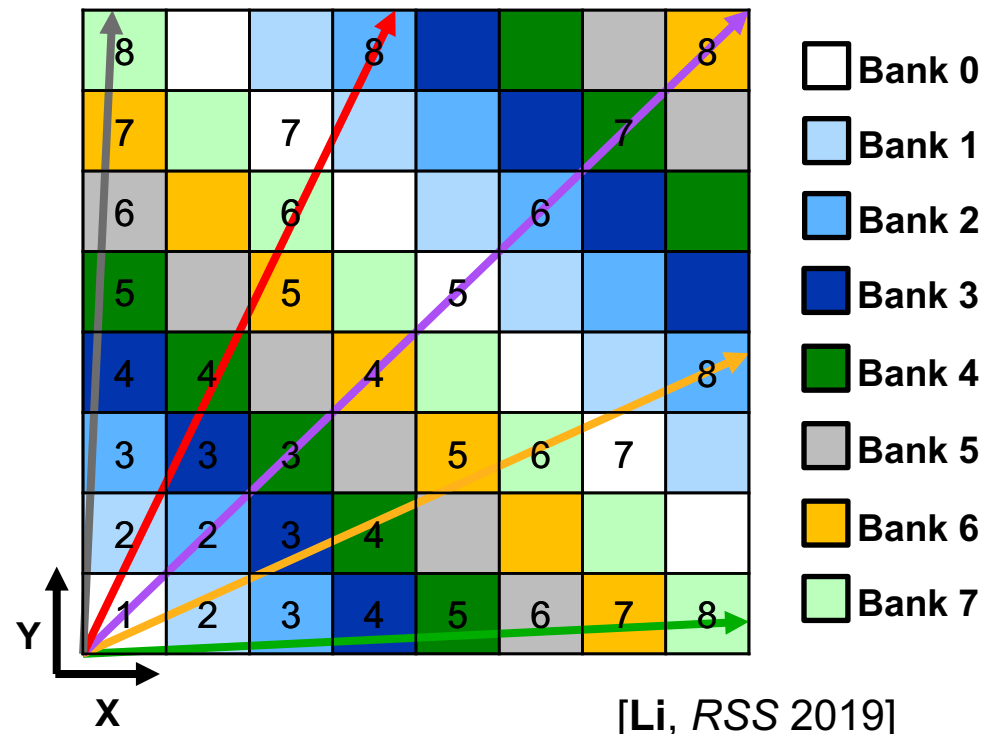
Specialized Memory Architecture

Break up map into **separate memory banks** and novel storage pattern to minimize read conflicts when processing different beams in parallel.

Memory Access Pattern



Diagonal Banking Pattern



Compute the mutual information for an **entire map** of 20m x 20m at 0.1m resolution **in under a second** → a 100x speed up versus CPU for 1/10th of the power.

Monitoring Neurodegenerative Disorders

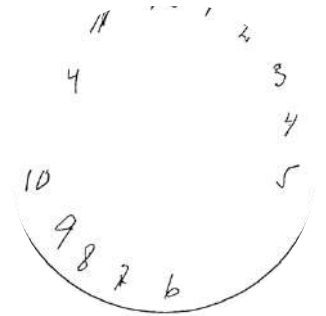


Dementia affects 50 million people worldwide today (75 million in 10 years) [World Alzheimer's Report]

Mini-Mental State Examination (MMSE)

- Q1. What is the year? Season? Date?
 Q2. Where are you now? State? Floor?
 Q3. Could you count backward from 100 by sevens? (93, 86, ...)

Clock-drawing test



Agrell et al.
Age and Ageing, 1998.

- Neuropsychological assessments are **time consuming** and **require a trained specialist**
- Repeat **medical assessments** are **sparse**, mostly **qualitative**, and suffer from **high retest variability**

Use Eye Movements for *Quantitative* Evaluation

Eye movements can be used to quantitatively evaluate severity, progression or regression of neurodegenerative diseases

High-speed camera



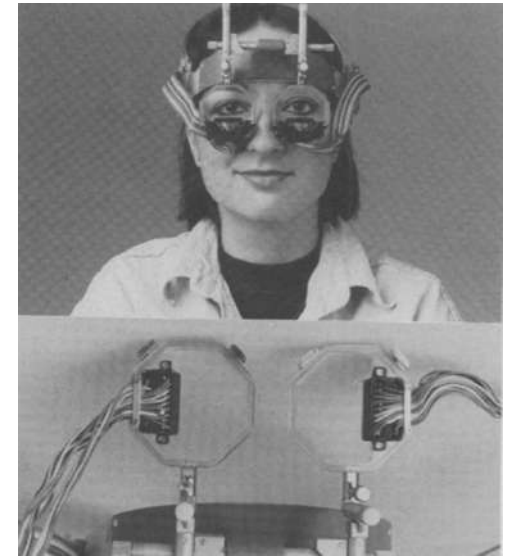
Phantom v25-11

Substantial head support



SR EYELINK 1000 PLUS

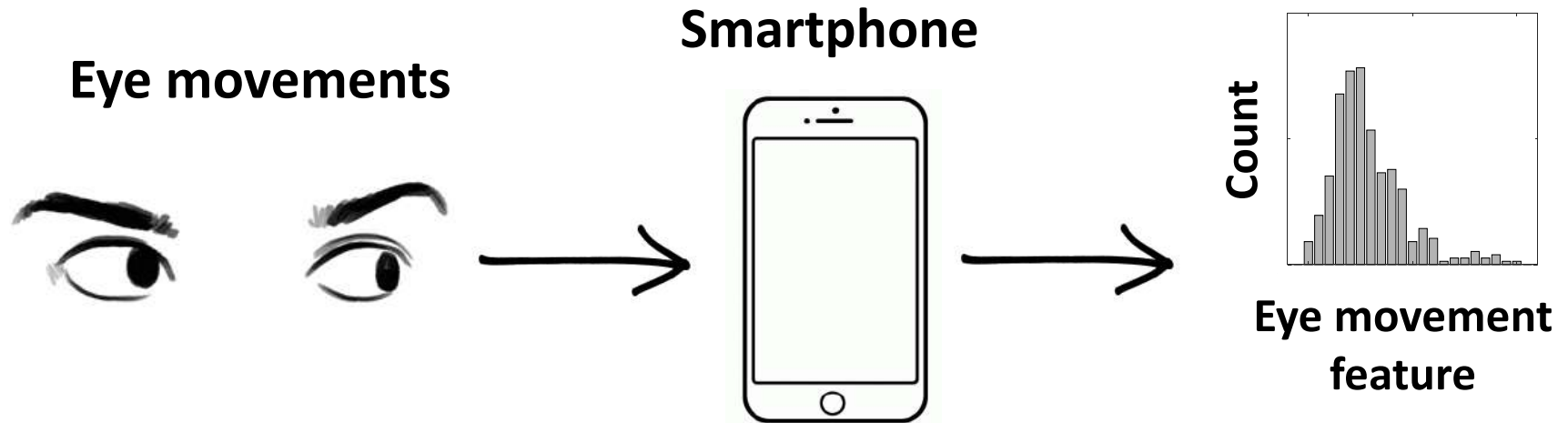
IR illumination



Reulen et al., *Med. & Biol. Eng. & Comp*, 1988.

Clinical measurements of saccade latency are done in constrained environments that rely on specialized, costly equipment.

Measure Eye Movements Using Phone



Develop algorithm to measure eye movement using a **consumer-grade camera** rather than high-cost research-grade camera.

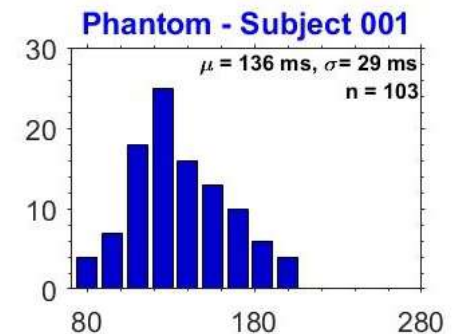
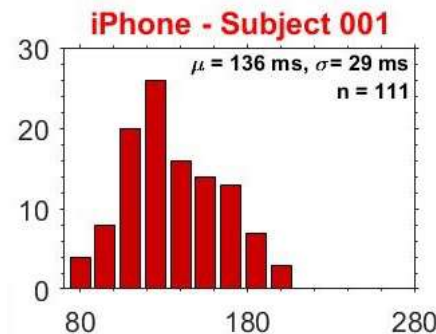
Enable low-cost in-home longitudinal measurements.



iPhone 6
($< \$1k$)



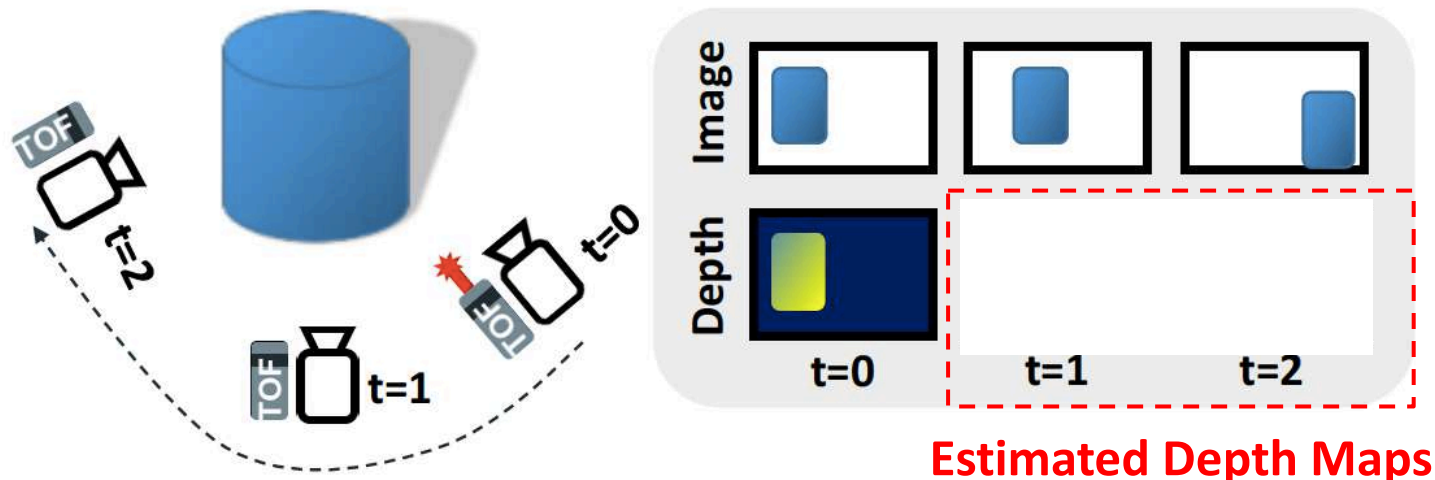
Phantom
(\$100k)



Reaction Time (milliseconds)

Low Power 3D Time of Flight Imaging

- Pulsed Time of Flight: Measure distance using round trip time of laser light for each image pixel
 - Illumination + Imager Power: 2.5 – 20 W for range from 1 - 8 m
- Use computer vision techniques and passive images to estimate changes in depth without turning on laser
 - CMOS Imaging Sensor Power: < 350 mW

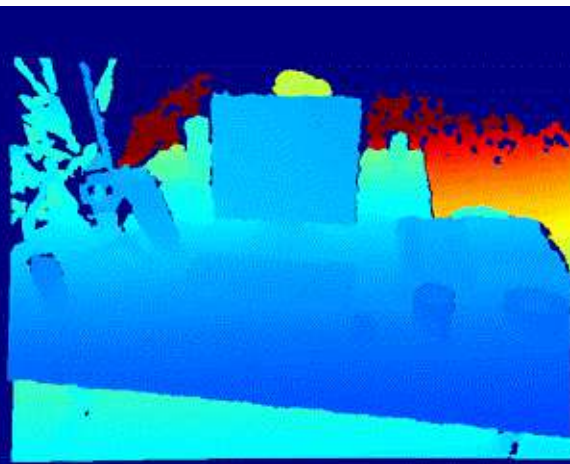


Real-time Performance on Embedded Processor
VGA @ 30 fps on Cortex-A7 (< 0.5W active power)

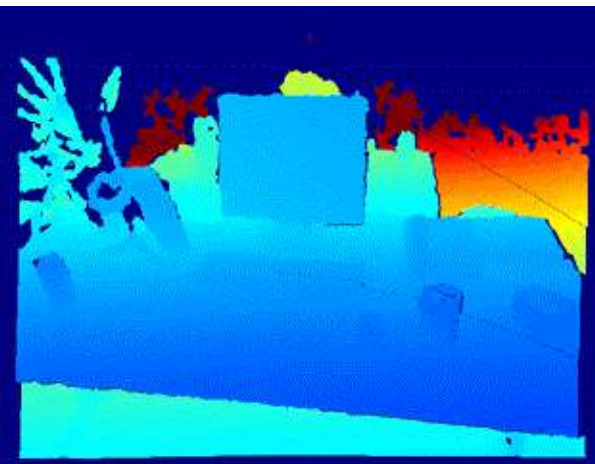
Results of Low Power Depth ToF Imaging



RGB Image



Depth Map
Ground Truth



Depth Map
Estimated

Mean Relative Error: 0.7%
Duty Cycle (on-time of laser): 11%

Summary

- Energy-Efficient AI extends the reach of AI beyond the cloud by **reducing communication requirements, enabling privacy, and providing low latency** so that AI can be used in wide range of applications ranging from robotics to health care.
- **Cross-layer design with specialized hardware** enables energy-efficient AI, and will be critical to the progress of AI over the next decade.

Additional Resources

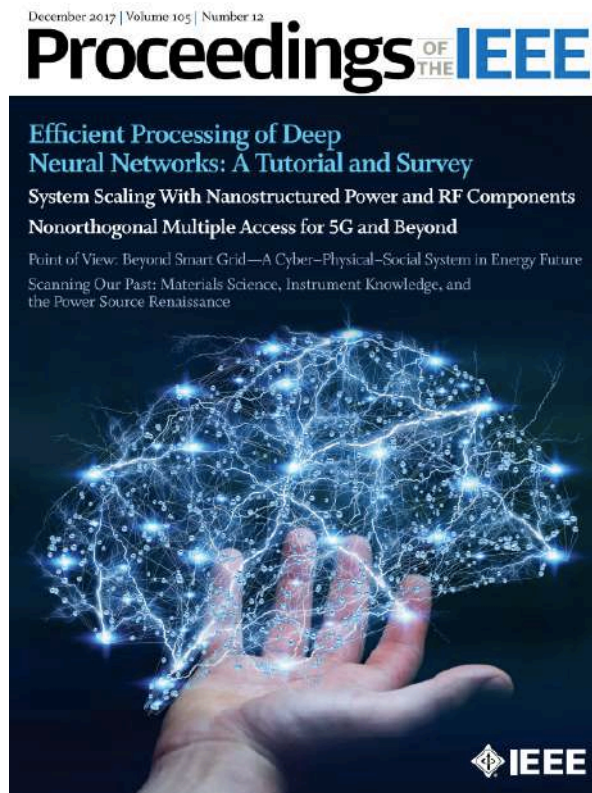
Overview Paper

V. Sze, Y.-H. Chen, T.-J. Yang, J. Emer,
“Efficient Processing of Deep Neural Networks: A Tutorial and Survey,”
Proceedings of the IEEE, Dec. 2017

Book Coming Spring 2020!

More info about
Tutorial on DNN Architectures

<http://eyeriss.mit.edu/tutorial.html>



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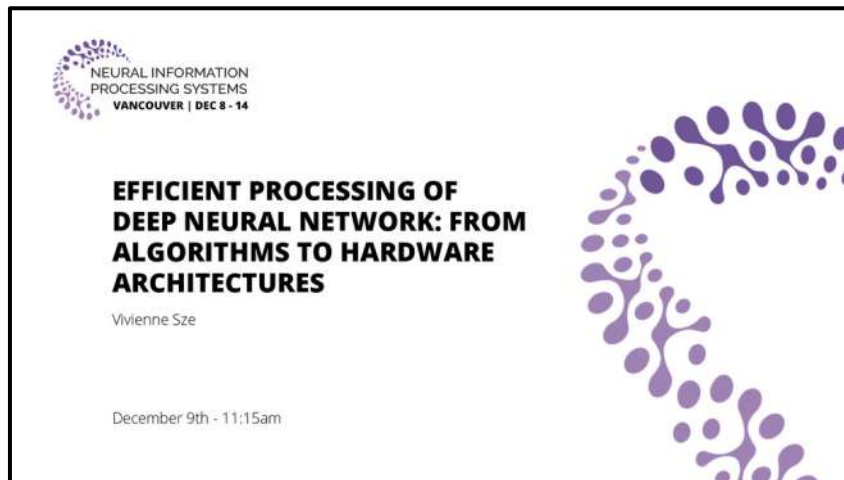
[http://shortprograms.mit.edu/dls](https://shortprograms.mit.edu/dls)

Next Offering: July 20-21, 2020 on MIT Campus

Additional Resources

Talks and Tutorial Available Online

<https://www.rle.mit.edu/eems/publications/tutorials/>



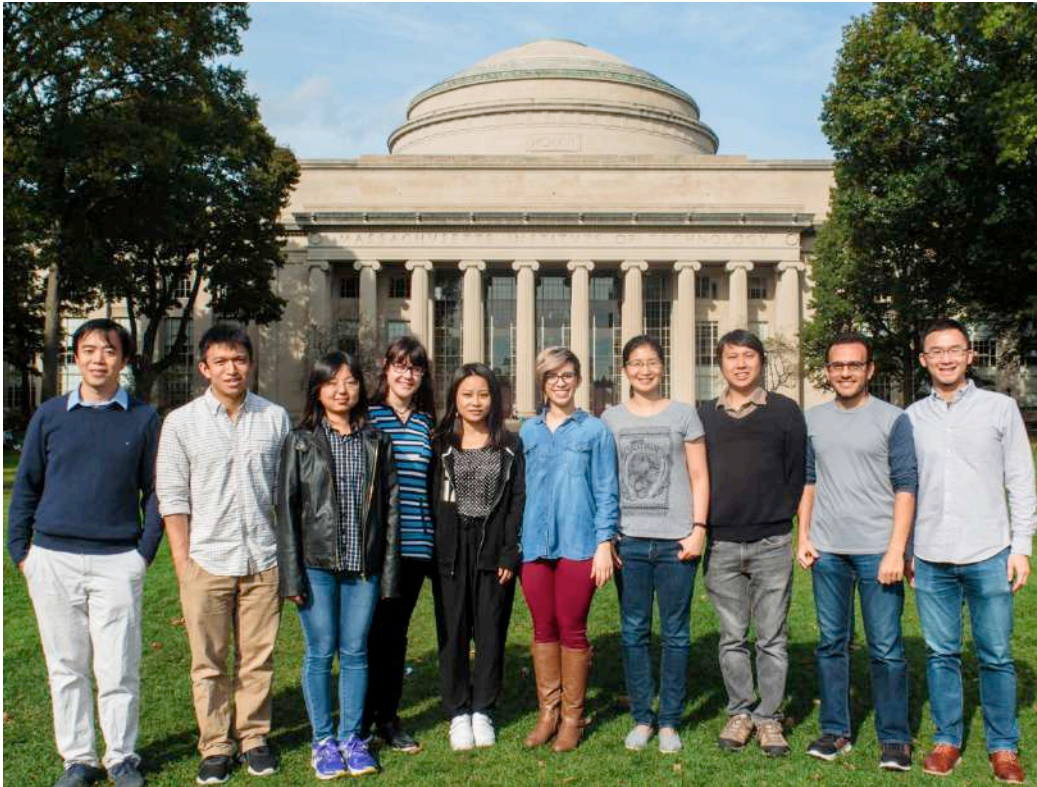
YouTube Channel

EEMS Group – PI: Vivienne Sze

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Acknowledgements



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