# High-throughput Computation of Shannon Mutual Information on Chip Peter Zhi Xuan Li<sup>\*</sup>, Zhengdong Zhang<sup>\*</sup>, Sertac Karaman, Vivienne Sze Massachusetts Institute of Technology

# 1. Introduction & Summary of Contribution

**Robotic Exploration** Where should the robot move next to learn the most about its environment?



### Challenge

Computing the mutual information I(M;Z) is **slow** (high time complexity) and thus becomes the **bottleneck** of autonomous exploration system.

# **Our Contribution**

Multicore mutual information (MI) hardware accelerator consisting of: 1) Specialized memory architecture

# 2. Autonomous Exploration Pipeline & MI Formulation



#### **Typical Autonomous Exploration Pipeline**

Occupancy Map Mutual Information (MI) H(M|Z) = H(M) - I(M;Z)

**Theoretically Proven Approach** Move to the location that **maximizes the** mutual information between prospective range measurements and the map.

- 2) Fast & fair arbiter
- 3) 16 high-performance MI cores

#### System Performance

Computes the mutual information for an entire map of 20m x 20m at 0.1m resolution in under a second while consuming under 2W on an FPGA

# 3. Hardware Architecture

### Challenge: Memory Bandwidth (Not Compute) Limits Performance

a) Algorithm is **highly parallelizable** across MI computation for every sensor beam



**Ideally**, each core computes MI for each beam using **its** own memory read port to independently access the map b) Standard, low power SRAM has only **two ports!** 



c) **Partition** and store the occupancy map into several memory banks to increase memory bandwidth



Specialized map partitioning pattern & arbiter are required to optimize data delivery to the cores

Data delivery, specifically **memory bandwidth** (not compute), limits the system throughput

#### **Proposed Solution & Detailed Implementation**

2. Round-robin arbiter **fairly and quickly resolves** 

memory read conflicts among cores

1. **Diagonal partitioning** of the occupancy map **minimizes** memory read conflicts among cores



Proposed Implementation: Bank 5 Example Naïve Implementation Priority 100 I 30 4 5 5 | | 30 | 4 | 7 | 5 |-Expected Window Size for Bank 5

### 3. High-performance mutual information cores using parallelized and pipelined internal operations



Note: Parameters (highlighted in red) needed for FSMI computation are generated by Look Up Tables using quantized occupancy value b<sub>i</sub> from the map

- P(e<sub>i</sub>), C<sub>k</sub> and I(M;Z) are executed in parallel while their individual operations are **pipelined internally**
- > MI for each beam is computed in **n+15 cycles**, where n is the number of cells in a sensor beam
- Final hardware system contains 16 cores

- > All cores access the same column or row of the map every cycle (left Figure)
- > Diagonal banking pattern **minimizes read conflicts** by making cores access different banks every cycle (right Figure)
- Naïve implementation (left Figure) executes in linear time **O(T)**, T = # of cores
- > **Proposed implementation** (right Figure) executes in logarithmic time O(log(T)+log(B)), T = # of cores, B = # of banks. (T=16, B=16 in our design)

### 4. Results

## 5. Extending MI Computation to 3D Environments

Ray

in OctoMap

Uncompressed input format

 $+ L_2 + L_3$ 

 $(o_1, L_1), (o_2, L_2), (o_3, L_3), \dots, (o_{n_r}, L_{n_r})$ 

Compressed format (Run Length Encoding)

 $., o_1, o_2, ..., o_2, o_3, ..., o_3, ..., o_{n_r}, ..., o_{n_r}$ 



Computing MI on a **3D map** requires a significant amount of storage and computation



#### **Compute FSMI on the Compressed 3D Map**



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A 3D environment featuring an arch, a giant cat, a box and a tree

3D OctoMap where color indicates the height of a voxel

Computing FSMI directly on a 3D OctoMap achieves an **acceleration ratio of 8**×

For more information, please see: Z. Zhang et al., FSMI: Fast computation of Shannon Mutual Information for information-theoretic mapping, arXiv 2019 http://arxiv.org/abs/1905.02238